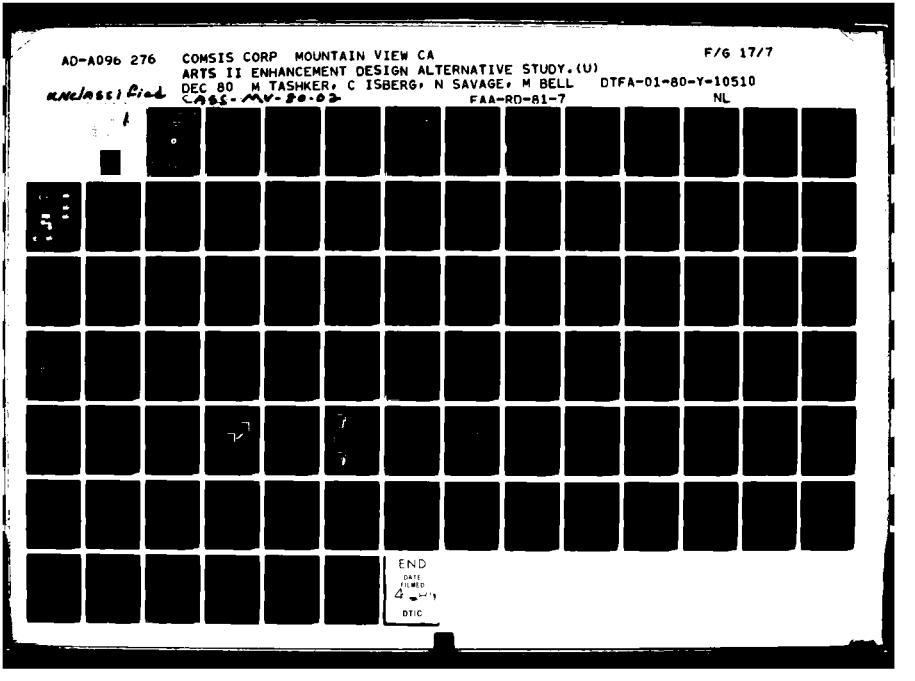
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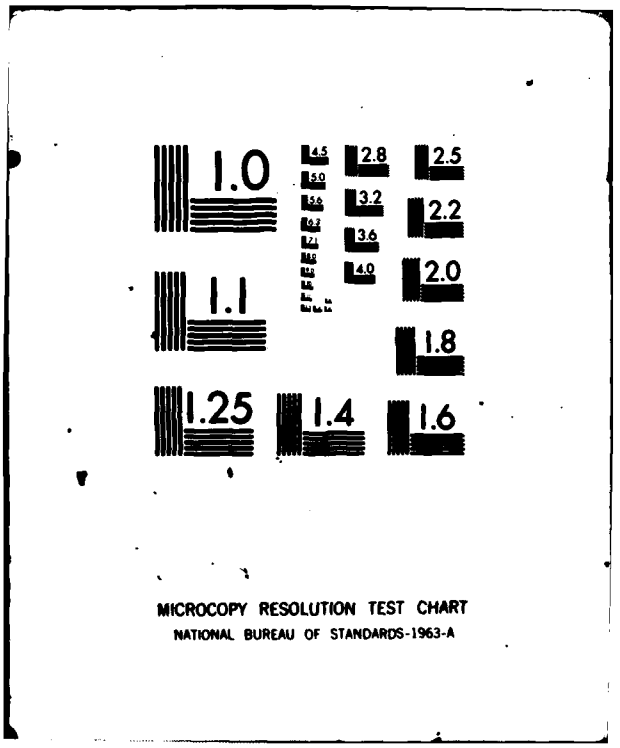
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16. Abstract

This report documents a study on an enhanced ARTS II, to be known as ARTS IIA. ARTS IIA will include the following features: beacon tracking, minimum safe altitude warning (MSAW), conflict alert, and training target generator (TTG). In addition, it will be compatible with various sensors and displays now under development, such as ASR-9, Direct Address Beacon System (DABS), and Tower Cab Digital Display (TCDD). The study considered the current capacity (memory and speed) of the ARTS II computer as well as the requirements for the near-term enhancements. Various computer configurations were investigated for cost, ease of system development, implementation, and installation. A recommendation is made that the current ARTS II computer be replaced with an LSI-2/40, a product of Computer Automation of Irvine, California.

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METRIC CONVERSION FACTORS

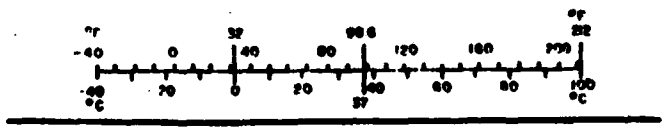
Approximate Conversions to Metric Measures

Symbol	When You Know	Multiply by	To Find	Symbol
	LENGTH			
in	inches	*2.5	centimeters	cm
ft	feet	30	centimeters	cm
yd	yards	0.9	meters	m
mi	miles	1.6	kilometers	km
	AREA			
in^2	square inches	6.5	square centimeters	cm^2
ft^2	square feet	0.09	square meters	m^2
yd^2	square yards	0.8	square meters	m^2
mi^2	square miles	2.6	square kilometers	km^2
	acres	0.4	hectares	ha
	MASS (weight)			
oz	ounces	28	grams	g
lb	pounds	0.45	kilograms	kg
	short tons (2000 lb)	0.9	tonnes	t
	VOLUME			
tsp	teaspoons	5	milliliters	ml
tbsp	tablespoons	15	milliliters	ml
fl oz	fluid ounces	30	milliliters	ml
c	cups	0.24	liters	l
pt	pints	0.47	liters	l
qt	quarts	0.95	liters	l
gal	gallons	3.8	liters	l
ft^3	cubic feet	0.03	cubic meters	m^3
yd^3	cubic yards	0.76	cubic meters	m^3
	TEMPERATURE (exact)			
°F	Fahrenheit temperature	5/9 (after subtracting 32)	Celsius temperature	°C

*1 in = 2.54 (exactly). For other exact conversions and more detailed tables, see NBS Misc. Publ. 286, Units of Weights and Measures, Price $2.25, SD Catalog No. C13.10:286.

Approximate Conversions from Metric Measures

Symbol	When You Know	Multiply by	To Find	Symbol
	LENGTH			
mm	millimeters	0.04	inches	in
cm	centimeters	0.4	inches	in
m	meters	3.3	feet	ft
m	meters	1.1	yards	yd
km	kilometers	0.6	miles	mi
	AREA			
cm^2	square centimeters	0.16	square inches	in^2
m^2	square meters	1.2	square yards	yd^2
km^2	square kilometers	0.4	square miles	mi^2
ha	hectares (10,000 m^2)	2.5	acres	
	MASS (weight)			
g	grams	0.035	ounces	oz
kg	kilograms	2.2	pounds	lb
t	tonnes (1000 kg)	1.1	short tons	
	VOLUME			
ml	milliliters	0.03	fluid ounces	fl oz
l	liters	2.1	pints	pt
l	liters	1.06	quarts	qt
l	liters	0.26	gallons	gal
m^3	cubic meters	35	cubic feet	ft^3
m^3	cubic meters	1.3	cubic yards	yd^3
	TEMPERATURE (exact)			
°C	Celsius temperature	9/5 (then add 32)	Fahrenheit temperature	°F



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EXECUTIVE SUMMARY

This report describes the results of a study undertaken to evaluate the available design alternatives for enhancing ARTS II capabilities. The study was performed in response to a desire to equip the ARTS II system with some of the safety enhancements currently operating at ARTS III AND IIIA sites and to enable the interfacing of ARTS II with various FAA systems under development.

The current ARTS II system provides automation for air traffic control at airports that handle a low to medium density of traffic. Alphanumeric flight data, presented on PPI radar displays, is time-shared with the normal radar display of primary and beacon targets. Automatic functions performed by ARTS II include identifying new beacon targets, associating those targets with previously entered flight plan data, and selecting a display format for each target on the basis of target status and type and the designated or requested controller display status. Other functions include managing display data, processing flight data or display requests, routing of ARTCC messages, and processing and reducing target input data from the radar beacon decoder.

The requirements for enhancement were divided into two categories: requirements and methods that were known or could be determined and implemented in a near-term time frame, and those that would be necessary to support systems and methods currently under development or planned for development.

The near-term enhancements for ARTS II are expected to build on current processing and display capabilities to provide additional functions. Specifically, the required near-term enhancements for ARTS II include:

- Safety monitoring for minimum safe altitude (MSAW).
- Safety monitoring for aircraft conflicts (CA).
- Beacon target tracking (required for MSAW and CA).

- Alarm notification and presentation to controller (aural and display data block).
- Target generation and simulation for controller training (TTG).

The functions and requirements for these features can be derived from similar capabilities implemented in the ARTS III operational systems currently used at airport facilities with high traffic densities.

This study considered the following requirements for future ARTS II enhancements:

- Redundancy for computer and other critical system components to provide fail-safe and fail-soft capability.
- Support for fully digital displays (e.g., FDAD, TCDD).
- Support for advanced sensor systems and processors (e.g., DABS, ASR-9, and SRAP).
- Capability to interface with other systems operating in the future air traffic control environment (e.g., TIDS).

The ARTS II computer, a Computer Automation LSI-2/20, is already heavily utilized for existing functions under heavy traffic and maximum configuration conditions; consequently, more capacity is required to perform the near-term enhancement functions. Although this computer adequately performs the currently required functions, it is limited in memory capacity and processing speed. This study was commissioned to investigate alternatives for expansion.

Recently, Computer Automation added the LSI-2/40 to its LSI series. The new model uses the latest electronic technology in the design of processor and memory components while providing architectural compatibility with the earlier LSI-2/20.

We recommend that the existing LSI-2/20 be replaced with the larger, faster LSI-2/40. With a simple chassis change, the LSI 2/40 can be installed in the same cabinet space as the LSI-2/20. Because this computer is upgrade-compatible with the current LSI-2/20, the current LSI-2/20 programs are expected to run without any modification on the new LSI-2/40. The existing I/O controllers and interfaces are directly compatible with the LSI-2/40. The LSI-2/40 provides up to 2.5 times the

speed and has a memory expansion capability of 1 million bytes. As configured initially, it will have 512,000 bytes of memory--four times that of the LSI-2/20.

The advantages of this recommendation are summarized as follows:

- This is the lowest cost alternative.
- This alternative can be easily implemented.
- The equipment can be easily installed, and the sites can be easily converted. That is, there will be no physical changes, no space additions, and little impact on operations.
- Early and rapid deployment of hardware is possible, independent of computer program development.
- There are qualified FAA and original system vendor personnel who can operate and maintain the system.
- This alternative is extensible; it can accommodate far-term requirements.

I INTRODUCTION

The Automated Radar Terminal System II (ARTS II) has been installed by the Federal Aviation Administration over the past 3 years to help control air traffic at low- to medium-traffic airports. As shown in Figure 1, ARTS II consists of:

- Data processing equipment contained in the acquisition process-cabinet (APC) in the facility's equipment room.
- A radar alphanumeric displays subsystem (RADS) in the IFR room.
- A BRITE alphanumeric subsystem (BANS) to interface with the BRITE displays in the tower cab.

The APC contains the Decoding Data Acquisition Subsystem (DDAS) and the computer. DDAS receives radar video responses from both broadband airport surveillance radars (ASRs) and air traffic control beacon interrogators (ATCBIs). Radar video (both primary and beacon) is presented on planned position indicator (PPI) displays. In addition, the computer presents a single symbol for each beacon-equipped aircraft and a two-line display tag containing the aircraft's identity and altitude. Other features include SPI and emergency flagging, hand-off procedure, automatic data block acquisition and termination, preview, Tab, and system display areas and interfacility communication.

To increase the safety benefits of the ARTS II system, there are plans to install some of the safety functions and features now operational on ARTS III. The near-term enhancements include conflict alert (CA), minimum safe altitude warning (MSAW), and training capability through a training target generator (TTG). In addition, MSAW and conflict alert require a beacon tracking routine, a display enhancement that allows three lines to be displayed in each full data block, and an external aural alarm.

Due to near saturation of the processor used for current operations, the inclusion of the near-term enhancements requires replacing or upgrading the CPU currently used.

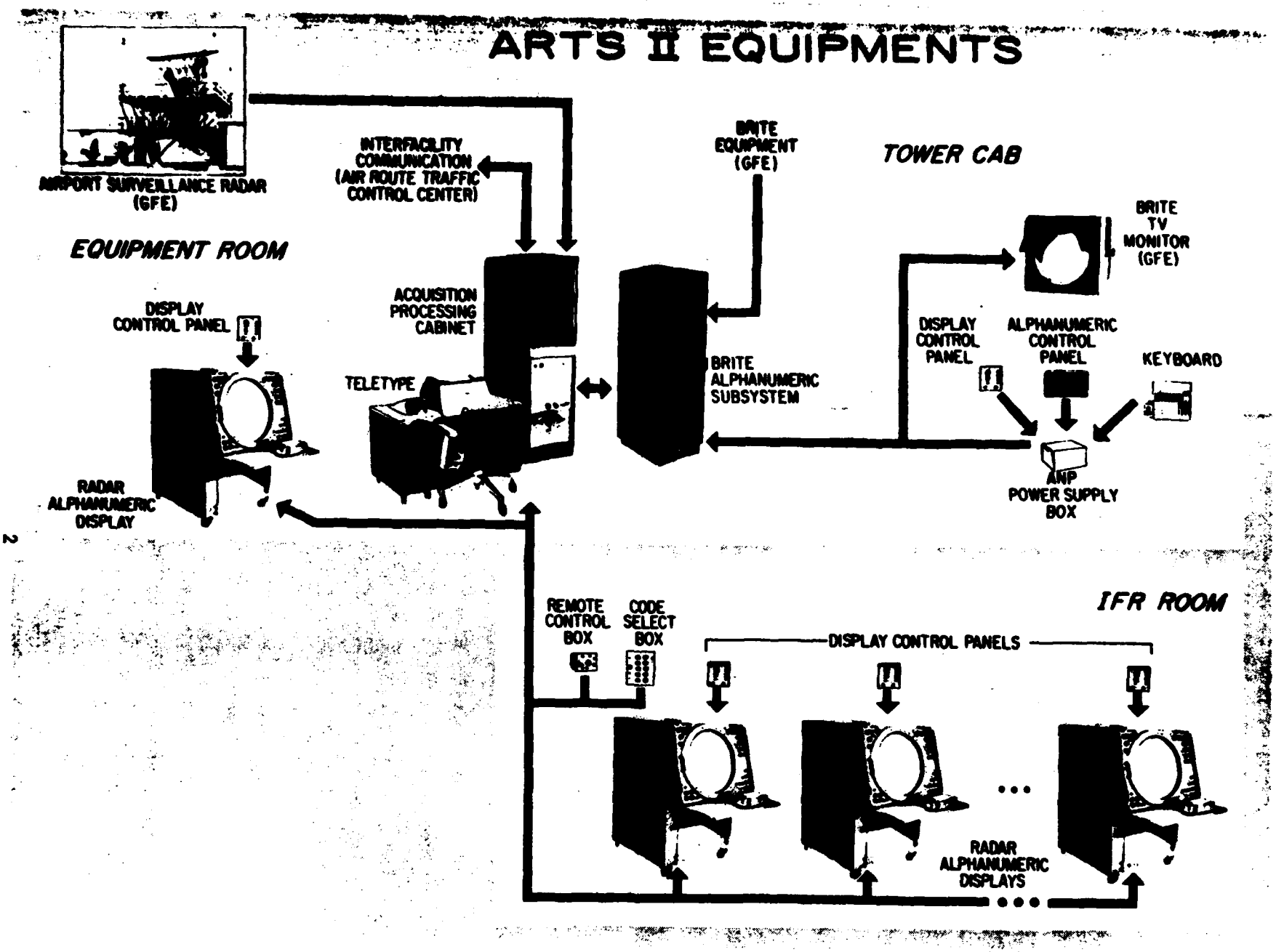


FIGURE 1 ARTS II EQUIPMENTS

Some far-term enhancements of ARTS II may also be needed. Eventually, ARTS II will have to interface with several ATC systems now under development, and may also require fail-safe or fail-soft capabilities. Examples of such systems include DABS, digital primary radar (ASR-9), SRAP (Sensor Receiver and Processor), and terminal information display system (TIDs). Full digital display capabilities will also have to be considered, such as those provided by the Full Digital ARTS Display (FDAD) and the Tower Cab Digital Display (TCDD). The ability to interface with such systems that are currently not in the field is designated as a far-term enhancement.

This study analyzed various design alternatives leading to both near- and far-term ARTS II enhancements. The technical advantages and disadvantages of each approach, relative life-cycle costs, and implementation strategies are considered.

Section II of this report discusses the current ARTS II system and, more specifically, those components affected by enhancements. The near-term safety enhancements are described in Section IV. Section V evaluates the advantages and disadvantages of each primary alternative (e.g., replacing the current computer with a larger, faster computer or adding smaller slave computers to the current computer). This section also evaluates the successive stages in each alternative's expected life (i.e., near-term safety enhancements, subsequent redundancy, later addition of digital displays and radars, and ultimate upgrade). Section VI analyzes the replacement of the current computer with the larger, faster, and code-compatible LSI-2/40. Costs and a development schedule are developed for this alternative. Advantages, disadvantages, and risks are described. Section VII discusses the 2/40 computer in a DABS-based future environment. Section VIII provides a summary and conclusions. Appendices are included to document performance specifications and air traffic projection.

II THE CURRENT SYSTEM

This section describes the current-system components that may limit future growth and estimates the extent of the limitations. Sections III and IV discuss the effects of specific enhancements on those components.

Major Components of the Current System

The major components involved in the enhancements are the DDAS, the computer, the I/O system, and RADS.

Decoding Data Acquisition Subsystem (DDAS)

During normal operations, DDAS does the following:

- Receives, qualifies, and decodes beacon video.
- Transmits (for further processing) digital words describing possible target replies to the computer.
- Supplies decoded beacon video directly to BANS and RADS.
- Incorporates provisions for generating and accepting beacon test video supplied by a source other than the ATCBI equipment.

At present, DDAS is designed to accommodate a number of possible targets per sweep (i.e., per ATCBI beacon pulse, which occurs approximately once per 2-1/2 to 3 milliseconds). Many responses can be received per sweep, ideally one response received per target aircraft in the sweep's path (approximately 3-4 degrees wide). The precise time at which the response is received, relative to the time the sweep was transmitted, is used to determine the target's range. The target's azimuth is determined by the angular position of the rotating radar antenna at the time the response was received. Target altitude may be decoded from a digital message transmitted by the target in response to the sweep. These data (azimuth, range, altitude, and identity code) are encoded by DDAS as digital words and transmitted to the computer. Although up to 30 sets of data, identifying 30 distinct targets, may be

sent from DDAS to the computer on each sweep, the number of targets is limited to 12-15 due to the design of the computer programs to the current computer's limited speed. This performance can be improved by replacing or upgrading the computer.

The Computer

The current ARTS II computer is an LSI-2 minicomputer produced by Computer Automation of Irvine, California. It features a 16-bit word format and 188 basic instructions. The printed circuit boards that constitute the computer are a processor full-board, processor half-board, option board, console board, and a number of 8K-word (core) memory boards--depending on site requirements.

The major functions of the computer include target declaration, display generation, and refresh; flight data input; and data entry control. The target declaration function processes the individual target response messages from DDAS and generates target reports for each beacon-equipped aircraft. Display generation and refresh functions format the alphanumeric display data and transmit it at a rate that provides flicker-free alphanumeric data displays on the RADS and BRITE displays. The flight data input function is responsible for maintaining an exchange of flight and position data to and from ARTCC and merging this data with the current ARTS II data base. The data entry control provides another method of entering or modifying information in the data base.

Input/Output (I/O) Controllers

Except for the teletype and console, the I/O of the LSI-2/40 computer consists of a number of I/O boards located in the DDAS chassis. Special controllers were developed and manufactured by Burroughs to interface with the display keyboard, magnetic tape, DDAS, and interfacility systems.

Radar Alphanumeric Display Subsystem (RADS)

RADS is a self-contained display system for a TRACON configuration. (The BANS synthetic data display is identical to the RADS synthetic data display, except that data are displayed on a 5-inch CRT instead of a 22-inch CRT. Thus, RADS can represent all current ARTS II display devices.) RADS presents radar, beacon, and map broadband data. It also gives computer-generated alphanumeric information. These data are presented on the controller's CRT. RADS is a time-shared device; alphanumeric data are sent from the computer via DMA channel during the "dead time" when broadband video are not being presented.

Synthetic data is presented on the RADS CRT by full data block (FDB), limited data block (LDB), or as a single symbol. Adding both MSAW and CA requires the addition of a third line in the FDB (similar to that currently used in ARTS III and IIIA) and a Tab line in order to present the visual alarm message. Section III describes the current information flow from computer to RADS, the method by which the third line will be transmitted, and possible formats for the three lines of data.

ARTS II Capacity and Sizing

At present, the computer may be fully utilized during heavy air traffic conditions at large ARTS II airports. By our calculations and Burroughs' benchmarks, the support of each display requires about 10% of the computer's capacity--7% for refresh processing and 3% for input-output with the maximum number of aircraft in the system. Although this capacity utilization indicates that the computer could support 10 displays at most, in practice a larger number have been supported (i.e., 11 displays at Pensacola, Florida--the heavy traffic loadings assumed do not apply at this airport). The heaviest traffic loading used to test ARTS II has been 212 aircraft and 44 flight plans. Six displays were used, and there were a maximum of 100 targets in any 45-degree in any sector. Burroughs' benchmarking effort estimated that an additional 81% of a computer's capacity would be required to process the near-term safety enhancement functions for this configuration and traffic loading.

The current ARTS II system allows a maximum of 11 displays and up to 64K words (128K bytes) of memory. The number of displays is limited in part by the amount of time required to refresh each display from the circular refresh buffer held internally in the computer. The current LSI-2/20 can be easily saturated at 11 displays with a moderate complement of traffic. The limitation on memory size stems from the addressing capability of the computer (15-bit addresses).

Appendix B contains a number of traffic estimates for current ARTS II sites in 1979 and 1990. This data provides some indication of the computer load increases expected in 10 years with the current configuration and no enhancements. Only a small number of sites are expected to have a capacity problem. We recommend a closer examination of growth estimates in relation to the expected near-term and far-term enhancements.

III NEAR-TERM ENHANCEMENTS

The near-term enhancements being considered for ARTS II are:

- Addition of a conflict alert algorithm (CA).
- Addition of a minimum safe altitude warning algorithm (MSAW).
- Development of a beacon tracking algorithm to serve both CA and MSAW.
- Addition of aural alarm notification and presentation (third FDB line and Tab lines) as required for CA and MSAW.
- Addition of a training target generator (TTG).

This section discusses these five enhancements from the point of view of the type of algorithm required (when there are alternatives) and the processing load that will be placed on the processor or DMA channel. First, the common components of both ARTS III and ARTS IIA* are discussed.

ARTS III Systems

The ARTS III system has evolved over a 10-year period from essentially an alphanumeric display processor similar to the current ARTS II, although it has greater input, processing, display capacity, and a beacon tracker. ARTS III, intended for use in medium-to-high traffic-density airport facilities, can accommodate a wide range of air traffic control environments (e.g., dual sensors, multiple primary airports). As a result, the ARTS III system (hardware and software) has been the vehicle for enhancements and developments. These include the following items, which represent current and some planned features of ARTS III and ARTS IIIA:

- Radar tracking (RBTL)--requires SRAP.
- Track-oriented smoothing tracking (ARBTL).
- Minimum safe altitude warning (MSAW).

---

*Designation of an ARTS II system with near-term enhancements.

- Conflict alert (CA).
- Enhanced target generator (ETG).
- Digital display output (FDAD, TCDD) (in development).
- DABS/ARTARS interface (in development).
- Metroplex airport facilities (e.g., New York TRACON) (near implementation).
- Remote/digital radar input.
- Continuous data recording (CDR).
- Multiple radar sensor inputs.
- Metering and spacing (in development)
- Data extraction/retrack.
- Multiprocessing, fail-soft/fail-safe.

ARTS IIA Components

The enhanced ARTS II system (ARTS IIA) can take advantage of the results gained over a period of years in developing and testing ARTS III features, and the best approach for achieving the most desirable results can be selected.

The major components of the ARTS IIA operational software that must be considered are:

- Supervisor and executive control
- Controller keyboard message processing
- Beacon radar input processing
- Beacon tracking and track store management*
- ARTCC/ARTS interfacility message processing
- Magnetic tape flight plan input processing
- Display output processing
- Minimum safe altitude warning*
- Conflict alert warning*
- Console typewriter message handling
- Training target generator*
- System data base.

---

*A near-term enhancement.

The following subsections discuss four major algorithmic enhancements, along with the third line addition to the FDB.

Tracking

Today traffic control systems use tracking processes that vary considerably in function, method, and organization. Generally, a tracker can include the following functions:

- Correlation of target report input from the sensor to active track data in the system.
- Smoothing of tracked position from reported position on the basis of track history.
- Computation of track velocity to be used for display and next scan prediction.
- Analysis of position deviation for detection of cross-track accelerations (turning).
- Processing of target reports not correlated with existing track data for purpose of display or track initiation.
- Prediction of track positions for next scan correlation on coasting of track position if no target report available.
- Update of position data for tracks being displayed.
- Processing of track being suspended or dropped from tracking.
- Association of tracking data with flight plans.

Of the various tracker implementations studied, the one that offers the best preferred performance, flexibility, and extensibility is that of ARTS IIIA. This is an ARBTL (augmented radar and beacon tracking level) tracker with the following features and characteristics:

- Early discrete code correlation.
- Track/report cross-referencing.
- Two-pass (primary and secondary) correlation.
- Turning and deviation trial processing.
- Optional automatic track initiation (track-all environment).
- Correction of position and velocity (slant) using track-oriented smoothing techniques.
- Next scan prediction of position.
- Update of track position and velocity for display on the basis of corrected calculation or last scan prediction (coast).

- Automatic association of new track with previously entered flight plan data.
- Automatic determination of tracks that should be dropped or suspended from further processing by the tracker.

As used in ARTS IIIA, the tracker described above represents a reliable and proven method that is compatible with the required safety features (MSAW and CA). The ARTS IIIA design documentation and program is a model that can be used as a basis for specification.

The ARTS IIIA tracker has several advantages over the others we studied; its highlights are given below:

- Early discrete code (EDC) processing eases processor load for the more complex and time-consuming cross-reference method.
- Cross-referencing (with EDC) is a proven technique that minimizes the possibility for track swapping.
- The cross-referencing technique is also compatible with the future possibility of radar tracking.
- Track-oriented smoothing is currently the standard method for correction in our traffic control systems because it gives better results for turn detection and prediction.
- It is possible to initiate tracking automatically on all tracks.

Currently, track-all capability is not required for ARTS II, but the design approach for the tracking programs should not preclude either manual or automatic track initiation. Because only associated targets will be eligible for MSAW and CA, the question of automatic track initiation is mainly one of operational convenience. Using current interface equipment, only beacon target information is available to ARTS II; hence, factors involving radar-only targets and radar-reinforcement of beacon targets need not be considered for purposes of determining capacity, timing, algorithmic method, or operation. This issue is expected to be resolved before perfoming a detailed design of the tracking program.

Minimum Safe Altitude Warning (MSAW)

The safety monitoring for minimum altitude is the most straightforward of the two safety functions considered for the near-term enhancements. MSAW was the first automatic safety monitor added to ARTS III and has been operating since 1976. The MSAW package recommended for

implementation in ARTS II should be based on the method employed by ARTS III.

Using aircraft position and speed information available during each scan, the monitoring function calculates whether an aircraft is getting too close to terrain or man-made obstructions. MSAW comprises three distinct types of monitoring. It determines approach eligibility and monitors approaches to the primary airport facility. This same eligibility and approach monitoring is also performed for any satellite airport facilities. If the aircraft does not qualify for these approach monitors, general terrain conflict is checked. Projected aircraft position over a 30-second period is also calculated and checked for altitude violations. If an altitude violation is detected, a warning is relayed to the controller by display message and aural alarm.

The data required by MSAW are:

- Aircraft position (X,Y)--obtained from beacon radar reports.
- Aircraft speed and heading--provided by the tracking models that have been tracking the target.
- Aircraft altitude (Z)--extracted from the Mode C beacon reports.
- Aircraft altitude velocity--obtained by an altitude tracker that is part of the tracking module.
- Terrain grid data showing the minimum altitude for each 2-mile square for all terrain to be covered by the MSAW monitor.
- Primary and satellite airport facility position, runway headings, capture ranges, altitudes, and inhibit areas.

Keyboard message processing must be provided in ARTS II for controller/MSAW communications. The alarm output from MSAW to the display would utilize a reformatted FDB and/or an additional (third) line appended to the two-line FDB format. There would also be one Tab line for each warning. This arrangement is estimated to be within the capability of the display hardware. Aural alarms would interface with the ARTS II computer by means of standard Computer Automation digital output attachment/control features that provide a simple method of program selection and control. The aural alarms themselves would be simple annunciators compatible with the digital output attachments.

A separate stand-alone program will be needed as part of the non-operational software library to enter, edit, and prepare the terrain map and other site-variable data required for MSAW; this could be adapted from the program used by ARTS III and should be coded using a high-level programming language. Use of the current ARTS III terrain map generators should be investigated.

Conflict Alert (CA)

The methods considered for performing CA in ARTS II were limited to those used by ARTS III conflict alert. Only controlled (associated, mode C equipped) targets are eligible for safety monitoring (CA and MSAW).

CA has been operating in ARTS III since 1977 and is the most complex function considered for the near-term enhancement of ARTS II. All track data requirements for MSAW apply to CA. CA converts the slant range positions and velocities used by tracking and display functions to ground plane (tangential plane at radar site) values. Altitude acceleration is employed in conflict projections.

Each CA-eligible aircraft is checked on every scan for potential conflicts with other CA-eligible tracks. A primary filter routine compares an aircraft's X-coordinate value with that of other aircraft, thus limiting the number of potential conflicts that need to be evaluated. A threaded list of CA-eligible tracks is maintained, by X-coordinate value, to save processing time in the primary filter program. If a potential conflict pair is detected by the primary filter, control is passed to a control program. The track pair is then evaluated for actual conflict by each of three separate algorithms. The three algorithms, each a separate program, will detect linear conflicts (LINCON), maneuvering and maneuver-sensitive target conflicts (MFMAMS), and proximity conflicts (PROCON).

Conflicts are detected by position projections and computation of minimum approach distances or common altitudes within the projection period. The computed values are compared against minimum separation

criteria, which are site variable and may vary according to conflict type and position (Airport Areas I-III). Depending on the type of conflict and the time remaining before minimum separation violation, an alarm will be declared immediately or after a required number of scans.

CA must be equipped with keyboard message processing to provide interaction between the controller and the processing modules. Operator action can inhibit any or all of the CA conflict types in the entire system, a particular controller position, a specific associated track, or a specific beacon code block.

Training Target Generator (TTG)

The training target generator (TTG) for ARTS II is not a safety-related function as such, but greatly enhances the training and qualifying of controllers. It allows the simulation of control situations that will rarely, if ever, arise in the operational environment and operates in conjunction with the on-line operational program to provide maximum availability and convenience for trainer, trainee, and operational personnel. TTG also provides for functional testing of operational programs. Standard training scenarios can be generated for tape input. In various documentation for ARTS III, this facility has been labeled enhanced target generator, training target generator, and integrated training target generator.

The recommended TTG program for ARTS IIA will perform three principal functions:

- TTG command message processing. This program interacts with the training keyboard and/or magnetic tape device and processes commands that: create, delete, and modify training target parameters; start and stop the training target updates; or inhibit the TTG functions.
- Training target maintenance. This program is a time-driven function that updates the training target data to simulate aircraft flight.
- Central track store update. This function injects the updated data for simulated targets into the processing stream to be handled by the operational software modules. This module should be driven by the operational programs and is the only interface between the ETG and operational software.

The recommended TTG features are as follows:

- The system will allow any unused display and keyboard positions to be assigned dynamically for training.
- The training operator will be able to direct the TTG program to accept and store training target data.
- The training target data will share storage space with operational target data but will be unmistakably intended for training use and display only.
- The processing of operational and training target data will be performed by the same modules and in an identical manner; however, there will be no interaction between the two types of data (e.g., no conflict pairing). Total segregation of targets will be maintained. That is, TTG targets will be used for training displays only, and operational targets will be used for operational displays only.
- TTG space in the central track store (or ARTS-II equivalent) can be preempted for operational program use at the expense of TTG.
- The entry and control of TTG data can be via keyboard or magnetic tape.

A training target capacity of 32 tracks seems adequate, although it may be desirable to provide a dedicated testing mode (no operational use) that would be limited only by the capacity of the central track store.

A separate off-line program will be needed as part of the nonoperational software to generate the training data scenarios for TTG if magnetic tape input is desired.

Since ARTS II installations do not usually maintain unused spare displays and keyboards, the necessity of a controller display/keyboard position for entry of TTG target commands could limit the use of TTG. Therefore, it is desirable to investigate the possibility of attaching a separate (less expensive) CRT/keyboard terminal or teletype unit for use with TTG.

Alarm Notification and Presentation

CA and MSAW require the display of alert messages in the FDB full data block of each involved aircraft. Additional information is displayed in a single Tab line. FDB information is sent to the display

hardware for analog display in the form of 32-bit messages of three types. Type-I messages give an X-Y position and a single symbol or Tab area. Type-II messages give a position and identify a full or limited data block. Type-III messages contain five 6-bit fields for the character symbols used in Tab areas and data blocks.

A sequence counter in RADS provides symbol positioning and generation and leader generation as required by Type I and Type II messages. Subsequent steps direct the character formatting until the receipt of new gross data.

When the display is formatting a full data block, the aircraft ID is displayed, and a carriage return follows automatically after the seventh symbol of the first line. Altitude alert symbols and a special designator are formatted on the second line. No automatic carriage return follows. If the data are directed to the left of the aircraft symbol, the display backspaces seven postions from the end of the leader to begin each line. Any data line with less than 7 characters is padded with leading or trailing blanks for proper justification.

A third data line can be added below the second line by sending additional Type-III messages. The first message must include a carriage return/line feed to reposition the cursor. The length of the second and subsequent lines is only limited by interference with the leader. The hardware limitation on data block display is 32 characters by 32 lines.

If the third data line is required to be displayed above the current first line (aircraft ID) as a 0th line, hardware changes will be needed. For this display format, a number of boards need to be replaced or rebuilt in each RADS and BANS at every ARTS II site. This change will require hardware engineering, board redesign, and substantial installation costs. The current price for similar boards of this size is approximately $1,000. The change is expected to involve two or more boards in each display. If these boards require replacement, it may involve the purchase of up to 1,000 new boards for displays and spares at a cost of over 1 million dollars.

The current ARTS III full data block format differs from the current ARTS II FDB format in the number of character positions and the addition of a third data line. The first line of an ARTS III FDB contains a 2- to 7-character aircraft ID followed by a 1-character CA/MSAW inhibit indicator (*, Δ, or +).

The second line contains up to 9 characters in three fields. The first field contains 3 characters. These characters are used for altitude or as a time-shared 3-character scratch pad. Altitude may be replaced by abbreviations for coast (CST), no ARTS track (NAT), ambiguous handoff (AMB), or invalid altitude (XXX).

A second single-character field indicates an assigned altitude, scratch pad, or a handoff recipient. The first two fields can also be used to display a beacon code.

Aircraft type uses up to 5 characters in the third field. This can be time-shared with ground speed or an alert symbol and followed by a special designator. Alert symbols include emergency (EM), radio failure (RF), departure message failure (DM), and unsuccessful interfacility transmission (IF). Special designators include identification (ID), heavy jet (H), VFR (V), and overflight (E).

The third or 0th line of an ARTS III format indicates MSAW and CA warnings. It consists of a blinking 2-character designator, either LA or CA.

Similar format conventions can be adapted for enhanced ARTS II data displays, but each line must be limited to 7 characters. The CA/MSAW inhibit indicator, now the eighth character in the first line, must be relocated. It can be displayed in the third data line when no warning is given.

The addition of the third data line and Tab line for each alarm will create an increased load on the displays. The maximum display load has been defined in the ARTS II system design data as shown in Table 1.

Table 1

MAXIMUM ARTS II DISPLAY LOAD

	Maximum No.	Clocks	Total
Full data blocks	12	332	3,984
Limited data blocks	39	215	8,385
Single symbols	161	72	11,592
Tab lines (10 characters)	4	227	908
Total			24,869

Each clock is .331 microseconds. The maximum display load requires 8,232 microseconds per refresh.

Each radar sweep (pulse) requires 699.8 microseconds of live display time. Therefore, the maximum pulse rate of 1,200 pulses per second (pps) requires 839,760 microseconds per second. This allows an acceptable refresh rate of 19.5 Hz with the maximum display load.

Each additional third data line of 7 symbols, for each aircraft with CA or MSAW, requires 117 clocks or 38.73 microseconds. Each Tab line requires 227 clocks (75.1 microseconds). If five pairs of aircraft are in conflict and 5 aircraft are at low altitudes, this will require an additional 15 third lines and 10 Tab lines. The maximum display load now requires 9,564 microseconds per refresh. With a pulse rate frequency (PRF) of 1,200 pps, the refresh rate would be 16.8 Hz. In some lighting, this rate may be unacceptable. If a refresh rate of 24 Hz is required, the PRF must be limited to 1,101 pps. A worst case of 10 CA pairs and 10 low-altitude warnings would allow a refresh rate of 14.7 Hz at 1,200 pps or a PRF of 1,055 pps at 24 Hz. The range of radar PRFs is 675 to 1,200 pps.

MSAW and CA enhancements require an aural alarm to alert individual associated controllers when MSAW/CA software detects a low-altitude or potential conflict situation. The aural alarm system will interface through standard Computer Automation I/O hardware or an equivalent facility.

IV FAR-TERM ENHANCEMENTS

The far-term enhancements being considered for ARTS II are:

- Interface with DABS
- Interface with TIDS
- Radar digitizing (SRAP)
- Display refresh offloading (using digital displays)
- Use of digital radars (e.g., ASR-9)
- Use of a "smart front-end"
- Redundant operation (fail-safe/fail-soft)
- Continuous data recording.

This section describes these enhancements and systems with respect to ARTS II.

Direct Address Beacon System (DABS)

DABS can provide ARTS with target reports similar to the SRAP system used at Tampa/Sarasota. DABS also contains a tracker designed to take advantage of the monopulse radars employed. The net effect on ARTS II would be to eliminate the need for much of the DDAS processing as well as the functions now performed by the SWEEP program, thus reducing the load on the ARTS processor. However, this effect cannot be assumed for any enhanced system design unless all ARTS II sites are within range of DABS sensors.

Terminal Information Display System (TIDS)

TIDS allows flight plan information to be input and changed by the radar controller without reference to flight strips. The TIDS processor is designed to act as an intermediary between terminal systems (ARTS II and III) and ARTCC. The mechanism of information exchange is an expanded repertoire of messages currently used for communication between NAS and ARTS. There will be some additional processing load on the ARTS CPU to

perform two functions: transmit and receive messages, and carry out instructions contained in the incoming messages. However, it is expected that the frequency of these requirements will be extremely low compared with on-line target processing requirements and can safely be ignored in planning computer requirements.

Sensor Receiver and Processor (SRAP)

SRAP provides digitized radar reenforced beacon target reports that can be transmitted by a modem or otherwise introduced to a CPU. This "off-the-shelf" hardware in production for the FAA can be easily procured and implemented at any ARTS II site. SRAP takes input from an analog radar (ASR-4,5,6,9) and beacon (ATCRBS). As installed at the Tampa/ Sarasota ARTS IIIA site, SRAP contains dual parallel Radar Data Acquisition (RDAS) and Beacon Data Acquisition Subsystems (BDAS) (Figure 2). Each subsystem requires a 16" (h) × 19" (w) × 25" (d) chassis. These subsystems receive radar and beacon video outputs and correlate sweep-to-sweep replies in order to produce radar and beacon target reports. These reports are then correlated in BDAS. SRAP also outputs weather reports.

Primary radar goes through a radar microprogrammed controller (RMC) box that does centroiding for successive sweeps and produces target reports. These reports are fed into the BMC box that does beacon centroiding for successive sweeps and also performs correlation with radar input.

BDAS consists of two hardware modules, a Beacon Extractor (BEX) and a Beacon Microprogrammed Controller (BMC) (Figure 3). BEX is similar to DDAS in the current ARTS II. It contains a signal processor that detects the leading edge of pulses and sends the azimuth, mode, range, code, and SPI to the BMC. BEX has a hardware defruiter and a video generator. The video generator can be used as an analog backup for the computer, which is also the case with DDAS in the current ARTS II.

BMC receives the BEX output, produces beacon target reports, and correlates these with RDAS reports. Beacon processing is performed on

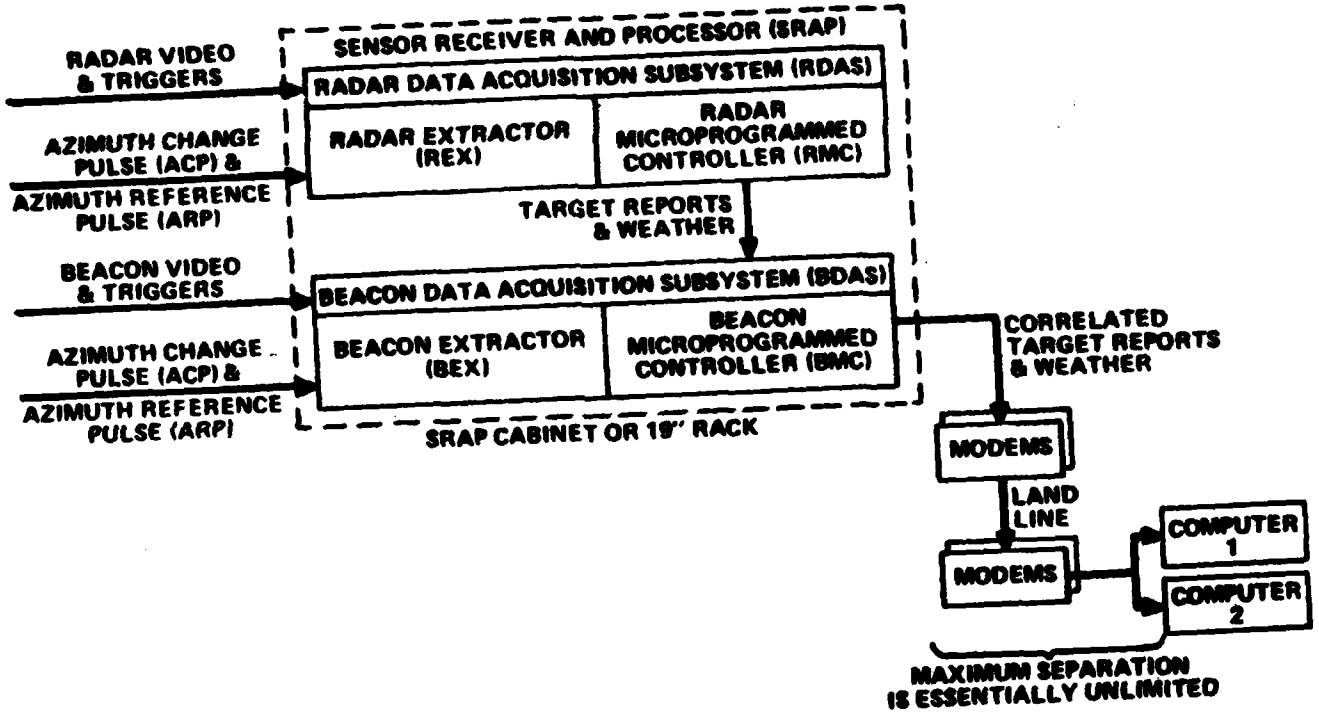


FIGURE 2 SRAP REMOTE INSTALLATION (STANDARD SERIAL INTERFACE)

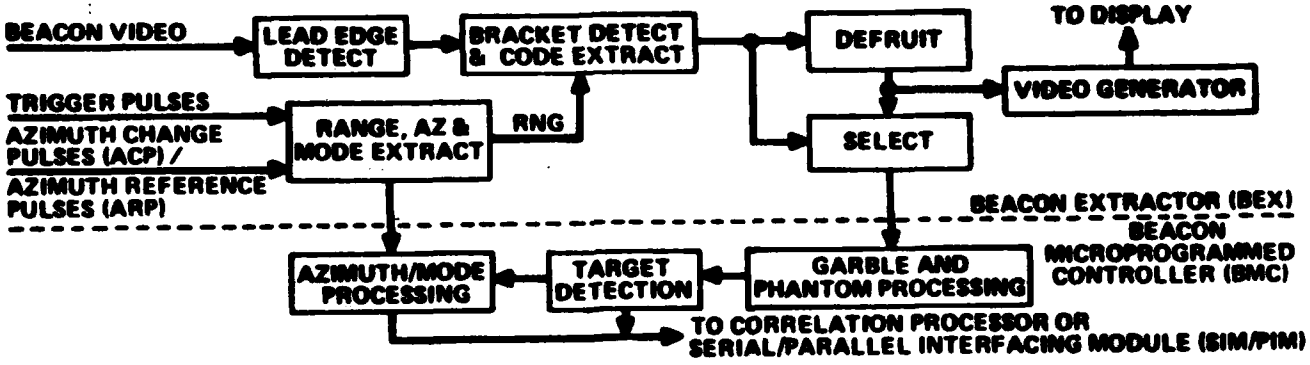


FIGURE 3 BEACON DATA ACQUISITION SUBSYSTEM

a time-sharing basis with the correlation and consists of alarm processing, garble detection, and sweep-to-sweep correlation. This processing is similar to the SWEEP program of ARTS II and outputs beacon target reports in an ARTS III format. BDAS can operate with a variety of Air Traffic Control Beacon Interrogators (ATCBIs), Series 3 through 5.

A Serial/Parallel Interfacing Module (SIM/PIM) can be used to assemble the SRAP output data in words of appropriate length and parity for serial or parallel transmission. Thus, no major problems would be encountered interfacing SRAP with an LSI-2/20 or 2/40.

Because there is no scan-to-scan tracking in the system, the radar reenforced target reports contain false alarms on the order of 130 per scan. This is reported to be a problem with the Tampa ARTS IIIA system.

The reported functions and capabilities of SRAP imply that it may be used in place of DDAS and the SWEEP program in ARTS II. To implement SRAP would require reprogramming the current ARTS II software so that SWEEP would become inactive and the Master Control Program (MCP) would be changed to recognize the beacon target reports arriving from SRAP through a normal I/O port.

SRAP can offload the SWEEP program from the APC processor. For a 6-display, 224-aircraft load, SRAP is estimated to free 23% of APC processor utilization (according to a Burroughs benchmark). This estimate includes the elimination of the current DMA load. The memory saved includes program storage of 871 words for SWEEP, data storage of 600 words, 3 beacon reply buffers of 80 words each, and the target detection file of 420 words. The current ARTS II program uses a 400-word target report file for output from the SWEEP program. This file is cleared by report processing every 45 degrees or half second. A DMA transfer rate of 400 words per half second requires less than 1% of processor utilization.

SRAP also provides greater reliability than the current DDAS it replaces. The MTBF of a BDAS is 7,825 hours, whereas DDAS is rated at 5,631 hours, and its capacity is more than 1,200 targets per scan. Because there is no requirement for radar/beacon correlation in the

near-term enhancements, only a single BDAS would be needed at a cost of approximately $30,000. Software modification would entail additional costs. A single BDAS in a SRAP cabinet can be easily upgraded to a full SRAP system with dual BDASs and RDASs. This would be advantageous when installing digital displays at ARTS II sites. With full digital output, SRAP could be located at the radar site and use lower cost phone lines to transmit data to the APC site. Therefore, no additional space would be required at the site.

Display Refresh Offloading

In the current ARTS II system, each display is refreshed up to 30 times per second from a refresh buffer file in the processor memory. The computer utilization used to create and update these files, along with the time spent completing the DMA data transfers, is significant.

The first solution is to develop an independent display refresh memory. The display refresh functions could be offloaded to this processor and memory. The second solution is to purchase digital displays to replace the current RADs. The design of TCDDs and FDADs includes internal display refreshing.

Computer utilization for display refresh processing consists of two functions. The first is the target display program, which refreshes each display refresh file from individual aircraft records. A refresh file contains display data only.

The second function requiring processor time is the DMA transfer of information from the refresh file to each display controller. This information transfer locks out the CPU from memory access for the duration of the transfer.

To estimate actual DMA utilization for a heavy traffic load, Burroughs completed a benchmark with 212 aircraft and 6 displays. The maximum amount of information displayed in any one display was 12 full data blocks, 38 limited data blocks, 161 single symbols, and 10 Tab lines of 10 characters each. In addition, each display displayed common system data, preview data, and PEM data. The number of words transferred

via DMA was as follows: FDB (96 words), LDB (234 words), SS (322 words), Tab (60 words), common data (30 words), system area (26 words), and preview area (26 words).

The Burroughs benchmark returned an estimate of 19.4% utilization for this loading of six displays. This result is close to an estimate of 3.5% per display for the time needed to transfer 734 words (30 Hz) at a DMA rate of 625,000 words per second. The Burroughs benchmark was also used to estimate the amount of computer utilization needed for the target display program. Their estimate is 36.4%.

If the target display function were offloaded, the actual aircraft files would have to be transferred to the display processor. The transfer must occur every half second because this information is updated every 45 degrees. These assumptions give a new estimated computer utilization of 1% per display. The total utilization savings is therefore 36.4%, plus 2 to 2-1/2% per display. The amount of memory saved is 1,849 words plus 678 words per display.

Further savings in DMA processor utilization may be attained by transmitting information only when a change has taken place. The full aircraft file of 3,328 words need only be transmitted once per scan, or every 4 seconds. This requires a processor DMA utilization of 0.1% per display. There could, however, be a concurrent increase in the processing required for program modifications. The central track store required for CA and MSAW in the near future will be larger. It can be accessed by quadrant to allow the transmission of current changes only. Additional DMA savings can also be made by sending only the changed data (altitude, X and Y position, velocity, alarm, etc.), but this will also require increased processing.

Radars

The ASR-9 development program is designed to produce a radar to replace ASR-4, 5, and 6. These three designs still use vacuum tubes, and approximately 200 of them are still in the field. The widely used ASR-7 is a transistorized magnetron unit with digital MTI as an output.

The ASR-8 is a klystron unit with digital MTI output. The ASR-9 will be a klystron unit with digital moving target detection (MTD) and a performance monitor.

Figure 4 shows a schematic block diagram of the ASR-9. The output of the high dynamic range receiver consists of two signals: inphase and quadrature. These are run into a 2-MHz digitizer driven by a finite impulse response filter. The output of the digitizer consists of range and Doppler responses, called primitives. These are run into a correlation and interpolation unit that outputs the centroid of target reports for each scan. These reports consist of range, azimuth, amplitude, Doppler, and the inevitable false alarm. False alarms are present on the order of 60 per scan. The reports are fed into an optional scan-to-scan correlator that reduces the false alarms to 2 or 3 per scan. After scan-to-scan delays, there is approximately a 90-degree or 4-second delay in processing these signals. The correlator output can drive a full digital display or be run through a display reconstituter for use on a time-shared display. Because of the amount of delay in the scan-to-scan correlator, the beacon video signal must be equally delayed. This requires the addition of a delay unit between the DDAS and the time-shared display.

In summary, the ASR-9 is a primary radar with an optional scan-to-scan correlator (tracker) that produces a digital output. This can be used to drive a full digital display, or it can be reconstituted to drive a time-shared display.

Front-End Processors

Advances in the development of microprocessors and memory may make it feasible to offload a large percentage of ARTS II programs into separate front-end processors. The modular structure of ARTS II programs and tasks facilitates the division of software among several machines. Such a processor, called a "Smart Font-End" (SFE), may be derived from the existing SRAP or from other efforts.

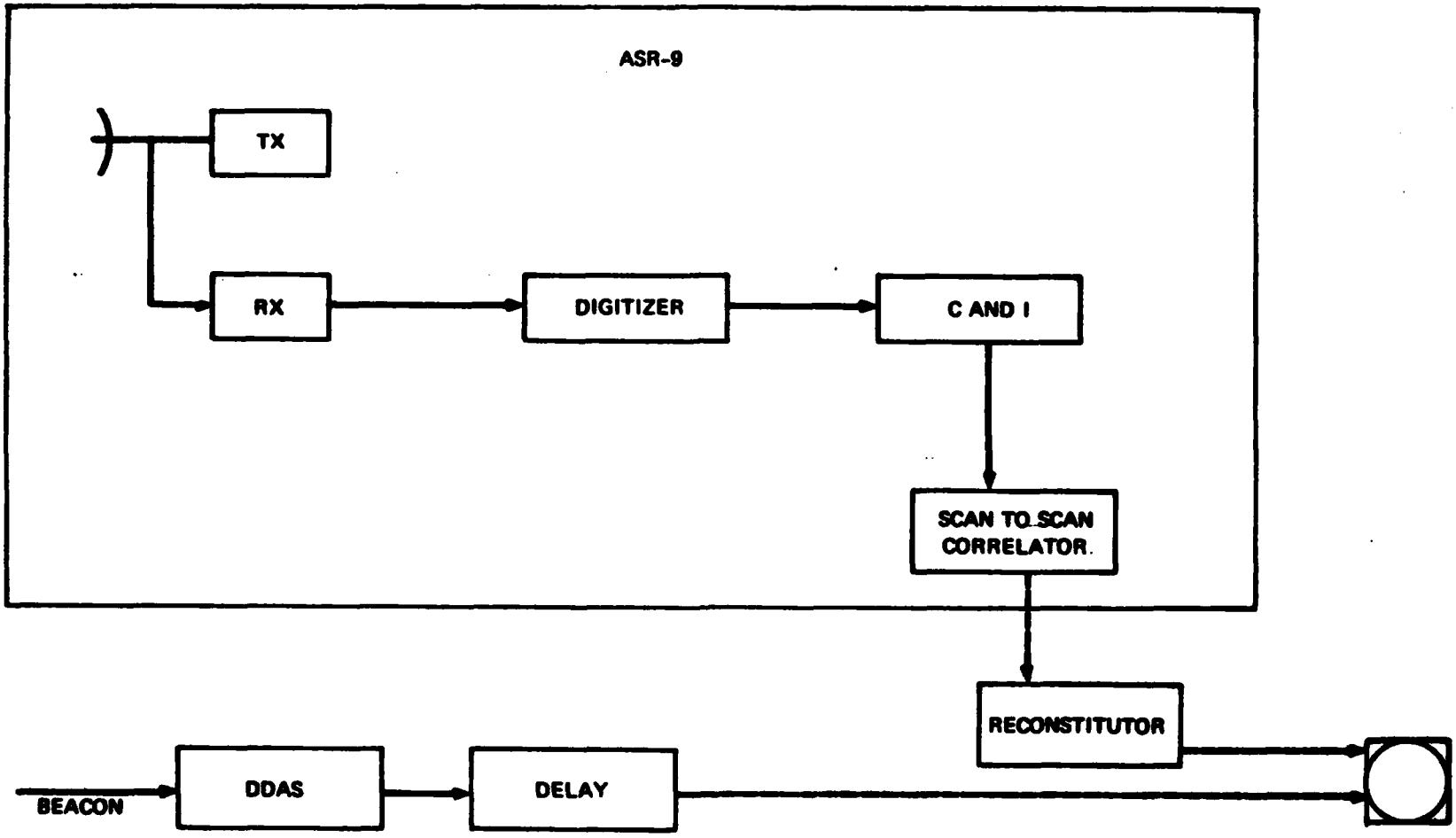


FIGURE 4 ASR-9 SCHEMATIC AND SCHEMATIC OF CONFIGURATION WITH TIME-SHARED DISPLAY

The goal of an SFE project would be to develop the software, hardware, and interfaces required for an all-digital front-end to provide digitized radar and beacon data acquisition, tracking, conflict alert, and MSAW. The 2/40 processor would act as a display and communications processor. The development effort required would be greater than the current ARTS II enhancement program. Current and near-term software would have to be completely redesigned for microcoding into firmware for microprocessors.

SFE would be expected to operate in an all-digital environment requiring both beacon and radar tracking. Implementation of an SFE system may follow the introduction of SRAPs or be implemented separately.

All R&D efforts in these areas should monitor the development of other ATC enhancement programs, such as DABS and the ARTCC 9020 replacement. These systems could affect ARTS II interfaces and communications and in some scenarios, eliminate the need for an SFE-type improvement.

Redundancy

Redundancy would require implementing additional or parallel processing units, with appropriate added software and switches, to improve system availability. Redundancy could improve safety performance by reducing the number of system failures and the resulting fallback to radar-only display output. Full parallel processing is usually designed to at least provide for the failure of any single unit without substantial degradation in function. A possible exception is momentary transient system failures during switchover following a failure. However, subsequent failures of additional units could result in degraded modes of operation or ultimately in complete system failure.

More important than the development of additional hardware, redundancy requires design of failure detection, switchover, and recovery software. Additional hardware is needed for system-to-system switching. In many redundant configurations, a common nonvolatile data medium such as disk memory is needed for recovery of data from the time of failure and for loading or reloading the appropriate operations system modules.

V EVALUATION OF PRIMARY ALTERNATIVES

This section describes, in qualitative terms, the evaluation of the primary alternative scenarios considered for the enhancement of the ARTS II system. The goal of this evaluation was to rank the alternative scenarios, eliminating those precluded by high life-cycle costs, severe technical risks, or unacceptable implementation or maintenance problems. The resultant ranking then became the basis of selecting Alternative 6, the replacement of the LSI-2/20 computer with the larger and faster LSI-2/40.

The objectives of this evaluation were to:

- Structure alternative life-cycle scenarios.
- Assess relative merits and associated problems of each alternative.
- Identify and provide critical data and analysis needed for decision.
- Rank alternatives, eliminating those precluded by high life-cycle costs or severe problems in development, implementation, or maintenance.

Table 2 is a summary comparison of the alternative capabilities. Each row represents a particular alternative, and each column represents a particular stage in the life cycle of the alternative. This section provides an increasingly detailed description of the alternatives, including a brief description of each stage of each alternative's life cycle with its associated merits and problems, and the disposition or ranking of the alternative.

The added equipment proposed for each alternative scenario and the ultimate disposition or ranking of each alternative is named in each row heading of Table 2. Because of the need for added computer capacity and speed for the near-term enhancements, the alternative scenarios are described in terms of the added equipment proposed for each. The columns

Table 2

SUMMARY COMPARISON OF ALTERNATIVES

STAGES / SCENARIOS (DISPOSITIONS)	I NEAR-TERM ENHANCEMENTS	II REDUNDANCY PARTIAL	II REDUNDANCY FULL	III DISTRIBUTION AND INTERFACE CAPABILITY	IV UPGRADE
1. ADD 2/30 (2 > 1)	Problems: Added Cabinet; Hardware Interface; Software Partitioning; Marginal Capacity	Provided	Impractical	Limited Capacity	Difficult
2. ADD 2/40 (6 > 2)	Problems: As Above, Except Merit: Capacity and Speed	Provided	Add DCAS, I/O, Add Switchover Recovery	Possible	Difficult
3. ADD REDUNDANT, EXTENDIBLE COMPUTER (6 > 3)	Problems: Logistics, Training, and Development; Incompatibility; High Cost; Additional Cabinets Merit: Long Range	Provided Within Redundant Computer	Not Available Except Long-Term	Possible	Extendible
4. ADD 4/100 (6 > 4)	Problems: Incompatible Languages; Limited Capacity and Speed, High Development Cost; Software Partitioning Merit: Existing Cabinet	N.A.	Duplicate APC, Add Switchover Recovery	Limited Capacity	Added Slaves (Bottleneck in 2/20)
5. ADD OTHER (6 > 5)	Problems: Logistics, Training Incompatibility; Functional Partitioning; Additional Cabinets	Could be Provided in "Other"	Duplicate All	Possible	Possible
6. REPLACE WITH 2/40	Preferred Alternative: Low Cost, Easiest Implementation; No Site Preparation; Compatible Software, I/O	N.A.	Duplicate APC; Add Switchover Recovery	Possible	Some Extendibility
7. REPLACE WITH REDUNDANT COMPUTER (6 > 7)	Problems: Disruptive to Existing Operations; High Hardware and Development Costs; Poor Match to Current Requirements	Provided	Provided	Possible	Extendible
8. REPLACE WITH OTHER (6 > 8)	Problems: Disruptive to Existing Operations; High Costs of Training, Logistics, and Redevelopment	Could be Provided	Could be Provided	Possible	Could be Extendible
8a. REPLACE WITH IOP (6 > 8)	Problems: High Cost of IOP; Disruptive to Existing Operations; Physical Space Merit: Minimum Software Development	Could be	Could be	Possible	Possible

of the matrix are labelled Near-Term Enhancements, Redundancy, Distribution, and Upgrade, and these are the successive development stages that must be considered for each alternative. The disposition or ranking of each alternative scenario, parenthetically shown in the row heading, simply identifies a superior alternative for each scenario (other than Alternative 6, which was judged to be the preferred alternative).

More specifically, the stages (columns) considered include:

(I) Near-Term Enhancements--MSAW, CA, TTG. These algorithms will require software modification and additions, but do not necessarily require substantial hardware changes except for the added computer capacity and speed required. CA and MSAW require tracking, a third display line, and an aural alarm.

(II) Redundancy--A configuration requiring additional or parallel processing units. Full redundancy precludes any loss of functional capability during the failure of any single unit. The failure of additional units may result in degraded modes of operation.

(III) Distribution and Interface Capability--Hardware and software modifications of the system to utilize ASR-9, SRAP, FDAD, TCDD, or DABS. SRAP and DABS may allow significant utilization reductions because of reduced sweep and target processing. FDAD and TCDD may allow significant utilization reductions because of reduced refresh and DMA requirements.

(IV) Upgrade--A long-term consideration that may include complete redesign or expansion to allow larger numbers of aircraft, displays, and features.

In making our recommendations, we considered such factors as development and site costs, existence of applicable software, and ease of implementation, as well as the more technical factors involving the ability of the equipment to handle the workload. One of the most important factors was the effect of equipment installation on ATC operations. We considered the actual interruption of operations for installing and testing new equipment, and physical factors such as available space in the facilities equipment room.

Scenario 1: Add LSI-2/20

The principal equipment change required for this scenario is the addition of a second LSI-2/20 computer to the current system. Because

there is little space left in the current APC cabinet, a separate cabinet would be required. It would be cable-connected, using DMA interfaces in both LSI-2/20 computers. The supporting software for this new interface would be developed for both computers, and the software for the enhancement functions would be developed primarily for the added computer.

Figure 5 summarizes the stages and disposition of this scenario. Although near-term enhancement can maximize the use of existing equipment and logistics, its associated problems are severe. The total CPU instruction execution capacity required, including near-term enhancements, was estimated at twice that of an LSI-2/20 for maximum configuration and air traffic requirements. Although the added 2/20 meets this capacity requirement, some added capacity would be required to support the intercomputer interface and the integration of safety calculations into the display processing. Similarly, the available memory capacity is marginal according to preliminary estimates. The interfacing and partitioning of functions between computers entails technical risks that cannot be fully assessed except through detailed design. The added complications will increase development costs and delays. The outdated design approach of the 7-year-old LSI-2/20 may cause problems and incur added costs in successive stages. Finally, the space and cabling required for the added cabinet will cause problems for some currently crowded ARTS II equipment rooms and require substantial front-end plant cost.

In the next stages, limited redundancy could be provided by adding switchover/recovery software and switches. If one of the 2/20s fails, this redundancy would allow the surviving 2/20 to resume processing at the current (non-enhanced) functional level. However, providing full redundancy (i.e., duplicating the APC, with the added 2/20, at each site) is impractical due to its high costs and the marginal capacity available for the added software required. Since this alternative has virtually the same cost as the next alternative but fewer capabilities, this alternative is definitely inferior.

I. Near-Term Enhancements:

Add an additional LSI 2/20 in a second cabinet

Develop near-term enhancement functions and interfaces

Merit: Maximum utilization of existing equipment, software, spares, and training

Problems: Marginal capacity and speed

Outdated design approach (hardware, software)

Additional plant cost complexity per site

Partitioning and interfacing cost and uncertainties

II. Redundancy:

A. Limited (fallback to existing functions)

Develop switchover/recovery hardware and software

B. Full

Add DDAS, I/O in second cabinet

Develop switchover/recovery system

Merit: Minimum cost for redundancy

Problems: Added expense, limited capacity

III. Distribution and Interface Capability:

A. Partial:

Develop added applications software as capacity permits

B. Full

Complete redesign, requiring different approach

IV. Upgrade:

Add additional 2/20s, 2/40s, or 4/10Ss in the added cabinet

Disposition:

The following alternative (Alternative 2), adding a 2/40, is superior to Alternative 1.

FIGURE 5 SCENARIO 1: ADD LSI 2/20

Scenario 2: Add LSI-2/40

This scenario entails the addition of an LSI-2/40 computer to the existing system in a manner similar to that described in Scenario 1. Because the 2/40 provides about 2.0-2.5 times the speed of a 2/20, for about the same cost, and up to 8 times the current memory capacity, it is clearly superior. In particular, the Scenario 1 problems of marginal capacity and speed and the outdated design approach are eliminated with the addition of the 2/40. These factors are summarized in Figure 6.

The later stages are similar to those previously described for the 2/20, except that full redundancy becomes practical if the existing 2/20 is replaced by another 2/40 (which then becomes identical to the redundancy stage of Alternative 6), and far more flexibility is available for the succeeding stages.

This alternative is decidedly inferior to Alternative 6. Additional costs include interface hardware, additional plant costs due to the added cabinet, and the development costs needed to develop the interprocessor interfaces and functional partitioning software. The problems of marginal capacity and outdated design approach associated with continued use of the existing 2/20 are retained.

Scenario 3: Add Redundant, Extensible Computer

This alternative, summarized in Figure 7, provides a modern design with excellent long-term capabilities by using advanced but currently available computer systems. For the near-term enhancements, an inherently redundant computer would be added to the existing system, and the software for the enhancements would be developed for the added computers by using a structured high-level language. However, the interface to the current computer and the functional partitioning would be as complex as for the preceding alternatives.

Although there are significant advantages to this approach, the problems far outweigh the advantages in the near term. Costs are high due to the hardware procurement costs for the added computers and expected plant costs to provide space for the additional cabinet. The

I. Near-Term Enhancements:

Add an LSI 2/40 in a second cabinet

Develop near-term enhancement functions and interfaces

Merit: Maximum utilization of existing equipment, software, spares, and training

Increased memory and processor capacity

Problems: Additional plant cost and complexity per site

Partitioning and interfacing cost and uncertainties

II. Redundancy:

A. Limited (fallback to existing functions)

Develop switchover/recovery hardware and software

B. Full (same as alternative 6 with redundancy)

Add DDAS, I/O in second cabinet

Additional 2/40 required to replace existing 2/20

Merit: Minimum cost to provide enhancements and redundancy

III. Distribution and Interface Capability:

A. Partial:

Develop added applications software

B. Full:

Redesign

IV. Upgrade:

Add more memory, slave processors, or 2/40s in the added cabinet

Disposition:

Alternative 6, replacing the existing 2/20 with a 2/40, is more cost-effective (due to the use of the existing cabinet and the existing software), provides equivalent growth paths, and does not retain the marginal capacity and other problems associated with the continued use of the current 2/20.

FIGURE 6 SCENARIO 2: ADD LSI-2/40

I. Near-Term Enhancements:

Add 2-Processor System to Existing APC

Develop hardware interface and enhancement software

Merit: High level languages, design approaches.

New design approach to enhancements leading to long range redundancy, distribution, and phase-out of current, limited computers.

Problems: Added costs per site (approx. 100K-200K for equipment)
Incompatible systems for development and maintenance
Added logistics, training
Difficult installation, may disrupt current operations
Additional equipment may require extensive site preparations
Software partitioning and hardware interface requires costly development

II. Redundancy:

A. Partial:

Integral within system

B. Full:

Reasonable for long term only

Let LSI 2/20 equipment atrophy

III. Distribution and Interface Capability:

A. Partial:

Develop distribution software and interfaces

B. Full:

Redevelop primary software

Phase out LSI 2/20, DDAS

IV. Upgrade:

Extensible, with additional processors

Disposition:

Other alternatives (e.g., Alternative 6) are much less expensive relative to the expected initial equipment cost of $100,000-$200,000 per site. The long-term advantages of this scenario are savings in software development (for redundancy and by virtue of high-level language and design approaches), but the projected savings, which are long-term and somewhat uncertain, are much less than the near-term and certain added equipment costs for all sites.

FIGURE 7 SCENARIO 3: ADD REDUNDANT, EXTENSIBLE COMPUTER

necessity of retaining the existing computer and software to avoid redeveloping the entire APC system and its interfaces, which would require the maintenance of two systems, is an additional disadvantage.

The merit of this approach increases in successive stages, but the certainty with which the projected cost savings in development can be attained diminishes with each successive stage, and the known near-term equipment procurement and expected site costs significantly exceed the anticipated savings. Large additional costs will be incurred for retraining FAA personnel. Also, the complexity of software partitioning and interfacing may counter any savings from high-level language software development.

Scenario 4: Add LSI-4/10S Slave Computers

This approach, summarized in Figure 8, adds a number of slave LSI-4/10 (single half-board) computers to the LSI 2/20 through DMA interfaces. The slave computer (4/10S) operates independently when it has requisite data and programs in its own memory. It becomes subservient to the main processor (a 2/20, 2/40, or processor of the LSI-4 series) when it requires unavailable data or when interrupted by the main processor. The slave may also interrupt the main processor to notify it of job end or request data. The slave resides on the DMA bus and is treated like any other controller. It relies on the same power supply as the main processor, but operating independently it will complete its tasks if a main processor failure is not catastrophic.

The slave computer uses the LSI-4 series instruction set. A translator is available that will translate up to 95% of normal instructions. Problems may occur if ARTS II programs contain many real time executive instructions since these cannot be translated and must be recoded. Although the LSI 2/20 can support up to four 4/10S processors, each added processor board reduces the available memory by one 8K board.

The interfaces and rudimentary systems software for this approach are available. Only the applications support for the enhancements, including the functional partitioning, need to be developed. The scenario

I. Near-Term Enhancements:

Add LSI-4/10S slave computers

Develop enhancement software and executive control monitor

Merits: Modular approach, low hardware cost, little or no system disruption

Problems: Limited capacity and speed available per slave
Each added 4/10S decreases the maximum amount of memory
Host 2/20 is limited, may become a bottleneck
Program partitioning uncertainties and incompatible assembly languages (4/10 vs. 2/20 increase development cost and delay

II. Redundancy:

Duplicate I

Develop switchover/recovery logic

III. Distribution and Interface Capability:

A. Partial:

Develop distribution software

B. Full:

Redesign -- different approach advisable

IV. Upgrade:

Addition of slaves is limited

Disposition:

Alternative 6, replacement of the 2/20 by a 2/40, is superior at a moderate added equipment cost of about $15,000 more per site relative to the basic equipment cost for this alternative. The problems and constraints listed above may be severe. An alternative approach to distribution is essential.

FIGURE 8 SCENARIO 4: ADD LSI-4/10S SLAVE COMPUTERS

would include full redundancy in its next stage at a moderate added development cost; however, the distribution and upgrade stages are less likely to be fully attained due to the extremely limited memory capacity and speed available in both the 2/20 and the 4/10 slaves.

The technical risks, which can only be fully investigated and assessed through a detailed design study, are severe. The slave computers each have only half the memory capacity and half the speed of the already limited 2/20 computers. It is estimated that at least three slaves would be required for the near-term enhancements. Further, it is estimated that the tracking and conflict-alert functions, which are closely interrelated, cannot be handled by a single slave computer under maximum air traffic configurations. If these two functions are provided by separate slaves, the interfacing problem is compounded since all communication between slaves must be directed through the already overloaded 2/20.

Development costs are expected to be high because of the partitioning required and interfacing problems. Consequently, this alternative was judged to be inferior to Alternative 6, which provides much greater capacity without the partitioning and interfacing problems.

Scenario 5: Add "Other" Computer

This alternative was considered for completeness. Computers from any of a number of available minicomputer lines--such as DEC's PDP 11 series, IBM's Series 1, or the 32 bit "supermini computers" available from DEC, SEL, or Perkin-Elmer--provide more memory capacity and speed than the LSI-2/40, but at a substantially higher cost. Other costs include: plant costs due to the additional cabinet, greater development costs due to partitioning and interface complexity, and maintenance and training costs due to unidentical systems.

As illustrated in Figure 9, the near-term merits of this approach are outweighed by the anticipated problems. Although the merits appear to increase in successive stages, they are uncertain and outweighed by the added costs of equipment, possible plant modification, logistics, longer development time, and uncertain hardware interfacing.

I. Near-Term Enhancements:

Add "other" computer

Develop interface and enhancement hardware and software

Merit: Modern design--structured high level
Development is separate from existing system

Problems: Incompatibility
Logistics, training
Added component may require plant improvements
Uncertain interfacing and software partitioning will result in higher development costs and longer delays

II. Redundancy:

Duplicate all equipment, develop switchover/recovery

Problems: Cost, complexity prohibitive

III. Distribution and Interface Capability:

A. Partial:

Develop additional software for "other" processor

B. Full:

Phase out LSI 2/20, DDAS

Redevelop primary software for "other"

Merits: A. Partial: additional software is in "other"
B. Full: preparation for eventual phase-out

IV. Upgrade:

Depends on upgradability of original "other"

Disposition:

Alternative 6 is superior, since the possible savings in software development appear minor relative to the added costs at all sites for equipment, site modification, training, logistics, and hardware/software. Depending on the added "other" computer selected, however, development and extension costs may be quite reasonable.

FIGURE 9 SCENARIO 5: ADD "OTHER" COMPUTER

Scenario 6: Preferred Alternative--Replace with LSI-2/40

This scenario, which would replace the 2/20 with the faster and larger 2/40, is summarized in Figure 10. The equipment changes required for the APC cabinet are minor and include: replacing the power supply (a larger capacity supply is required with a battery backup for the semiconductor memory), replacing the chassis (the current 2/20 motherboard must be replaced by a 9-slot split mother board), and adding the LSI-2/40 processor board, the memory mapping and cache board, and a 256K-byte memory. The current I/O interface boards in the DDAS chassis would be retained. This is by far the easiest scenario to implement and requires no additional site preparation, space, or plant costs. The substitution can be completed quickly and can be independent of software changes, thereby providing immediate relief from memory and speed limitations at some sites. No modification need to be made to other components when the 2/20 processor is replaced; the 2/40 is completely compatible with the current I/O and DDAS and fits into the existing cabinet.

The software for the enhancement functions would have to be developed, but since it would reside with existing software in the 2/40 processor, there would be no interfacing and partitioning problems. Thus, this alternative has the lowest software development costs of any scenario and the quickest implementation schedule. The processor has a FORTRAN compiler available to speed development; a decision on its use requires in-depth study.

This scenario's minimum cost and lack of site disruption appear unassailable, but there are still some associated risks involving availability and support. These are discussed in Section VI.

Scenario 7: Replace with Redundant, Extensible Computer

This alternative (Figure 11) provides a modern, high-level structured design approach to the ARTS II computer system and its interfaces. Although redundant extensible computers are available, they are oriented to commercial transaction processing and do not provide the real-time

I. Near-Term Enhancements:

Replace LSI 2/20 with LSI 2/40 in same cabinet

Develop additional software for enhancements (FORTRAN?)

Merits: Minimum cost site complexity code
Compatibility, and physical compactness with current cabinet, DDAS, and I/O
Little or no system disruption or plant cost
Immediate speed and memory relief
Easiest/quickest software development and system implementation

Problems: Risks in availability and support for the 2/40
Risk of 2/40 capacity

II. Redundancy:

Duplicate I and develop switchover/recovery hardware and software

III. Distribution and Interface Capability:

A. Partial:

Develop distribution software and interfaces

B. Full:

Phase out original software and interfaces, DDAS

IV. Upgrade:

Some extensibility

Disposition:

Best primary alternative

FIGURE 10 SCENARIO 6: REPLACE WITH LSI-2/40

I. Near-Term Enhancements:

Replace LSI-2/20 with redundant, extensible computer

Completely redesign primary software and interfaces

Develop additional software for enhancements

Merits: Redundant and extensible

Problems: High equipment cost ($100,000-$200,000 per site)
Not designed for current requirements
All software must be rewritten
Difficult logistics and training interfaces hardware
Equipment may require extensive site preparations
Implementation is costly and disruptive to existing operators

II. Redundancy: Viable only with full distribution

III. Distribution and Interface Capability:

A. Partial: Not viable

B. Full: Redesign primary software

IV. Upgrade: Provided via extensibility

Disposition: Cost and implementation make this inferior to Alternative 6

FIGURE 11 SCENARIO 7: REPLACE WITH REDUNDANT, EXTENSIBLE COMPUTERS

beacon processing capability or the RADS display interfaces. To provide these capabilities, the appropriate systems software for the replacement computers would have to be developed, in addition to redeveloping the current system, its interfaces, and the enhancement functions. These requirements add substantial development costs and delays to an already high hardware cost. Other disadvantages include: possible plant modifications to accommodate additional hardware; retraining costs; and lengthy and disruptive installation and cutover. Consequently, this alternative is inferior to Alternative 6.

Scenario 8: Replace with "Other"

This scenario, summarized in Figure 12, postulates the replacement of the LSI-2/20 computer with a larger, faster computer, such as the "supermini computers" available from DEC, SEL or Perkins-Elmer. The capabilities of such supermini computers exceed the requirements, however, and the advantages of a modern design approach are attainable only at the cost of redeveloping the entire system including its software and interfaces. Other disadvantages include plant costs and an installation process that would disrupt existing operations. Since the costs significantly exceed those of Alternative 6, the latter is decisively preferred.

Scenario 8a: Replace with the IOP

A significantly different scenario replaces the 2/20 with the IOP processor and software currently used in ARTS III sites. Since this IOP is compatible with DDAS and is already equipped with the enhancement functions, the development expense is almost entirely avoided. However, to interface with RADS and BANS, a new I/O board would be required. Other significant problems include: high equipment costs ($500,000 per site), physical space limits at ARTS II sites, disruptive installation, outdated technology, and the defacto upgrading of ARTS II sites to ARTS III. In view of the higher equipment costs and installation difficulties, this alternative is inferior to Alternative 6.

I. Near-Term Enhancements:

Complete redesign of primary software, interfaces

Utilize structured design

Merit: Modern design

Problems: High cost, long development time to rewrite software
Incompatibility with existing equipment (DDAS, displays)
Possible plant costs/site preparation
Logistics, training
Implementation is costly and disruptive to existing operations

II. Redundancy:

Duplicate I

Develop switchover software

III. Distribution and Interface Capability:

A. Partial:

Develop distribution software, interfaces

B. Full:

Phase out original software and interfaces

IV. Upgrade:

Depends on extensibility in original design

Disposition:

Alternative 6 is superior because of high costs and difficult implementation.

FIGURE 12 SCENARIO 8: REPLACE WITH "OTHER"

VI THE PREFERRED ALTERNATIVE

Replacing the current LSI-2/20 processor with the LSI-2/40--the newest Series 2 processor from Computer Automation--was chosen as the preferred alternative for several reasons, including:

- Hardware and software compatibility for rapid development, implementation, and deployment.
- Improved system capability.
- Low cost.

Compatibility

The LSI-2/40 has been designed to be compatible with Computer Automation's Series 2 computers. The equipment substitution, schematically illustrated in Figure 13, requires a minimum number of steps and little downtime. These steps are summarized in Figure 14 and illustrated in Figure 15. Because the 2/40 processor is compatible with current operational software, it can be installed without the safety enhancements. Hence, sites with current memory or processor saturation can be updated quickly while enhancement software is being developed.

The planned implementation requires no equipment-room modification, no additional power, and no additional air conditioning. The similar computer architecture requires only small changes in maintenance training.

Capacity

The speed of the LSI-2/40 is expected to be between 2 and 2.5 times that of the LSI-2/20 on the current application. Each memory board can contain 256K bytes; the older boards were limited to 32K-bytes. The memory mapping of the memory unit extends the memory addressing from 64K bytes to 8 million bytes. Without expansion, the 9-slot chassis has space for four memory boards, 1 million bytes, or eight times the current capacity of 64K words.

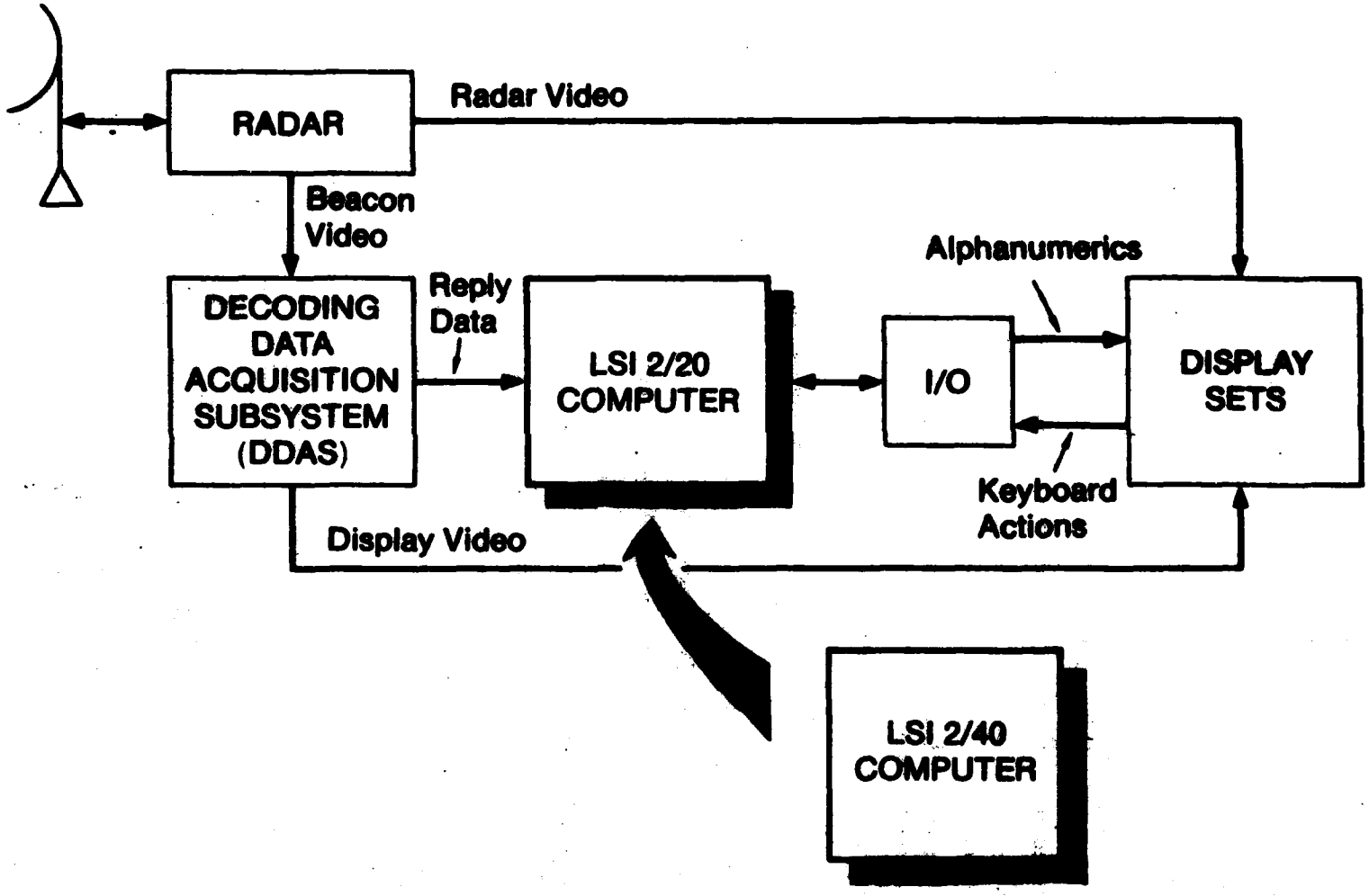


FIGURE 13 ARTS IIA COMPUTER SUBSTITUTION

ESTIMATED CONVERSION TIME

Change Equipment: 1-4 hours

Initial Operation (Diagnostic/Operational Program): 15 minutes

DETAILED CONVERSION STEPS

(1) Turn off APC and shut off (open breaker) on the primary power to APC.

(2) Unsnap computer console front panel and unplug console cable for computer mother board. Unplug I/O cables.

(3) Disconnect (screw lug terminals) power supply cable from computer.

(4) Remove LSI-2/20 chassis mounting screws (front of APC) and slip chassis out front of APC.

(5) Disconnect (screw lug terminal) computer power supply primary power cable from APC primary power distribution terminal block.

(6) Disconnect (plug connector) power supply cable from computer power supply.

(7) Remove computer power supply (mounting screws on front of APC) cover.

(8) Remove computer power supply (screws on front of APC).

(9) Remove power supply cable and replace with LSI-2/40 cable.

(10) Mount 2/40 power supply (includes battery backup unit).

(11) Replace computer power supply cover.

(12) Connect power supply cable (plug connector) to power supply.

(13) Connect power supply primary power cable (terminal lugs).

(14) Mount LSI-2/40 chassis (screws on front of APC).

(15) Connect power supply cable (screw lug terminals) and I/O cables.

(16) Reconnect computer console front panel cable to 2/40 mother board and snap in panel.

(17) Turn on APC (primary breaker) and run existing diagnostic program and then existing operational program.

FIGURE 14 CONVERSION STEPS TO REPLACE ARTS II LSI-2/20 COMPUTER WITH THE LSI-2/40

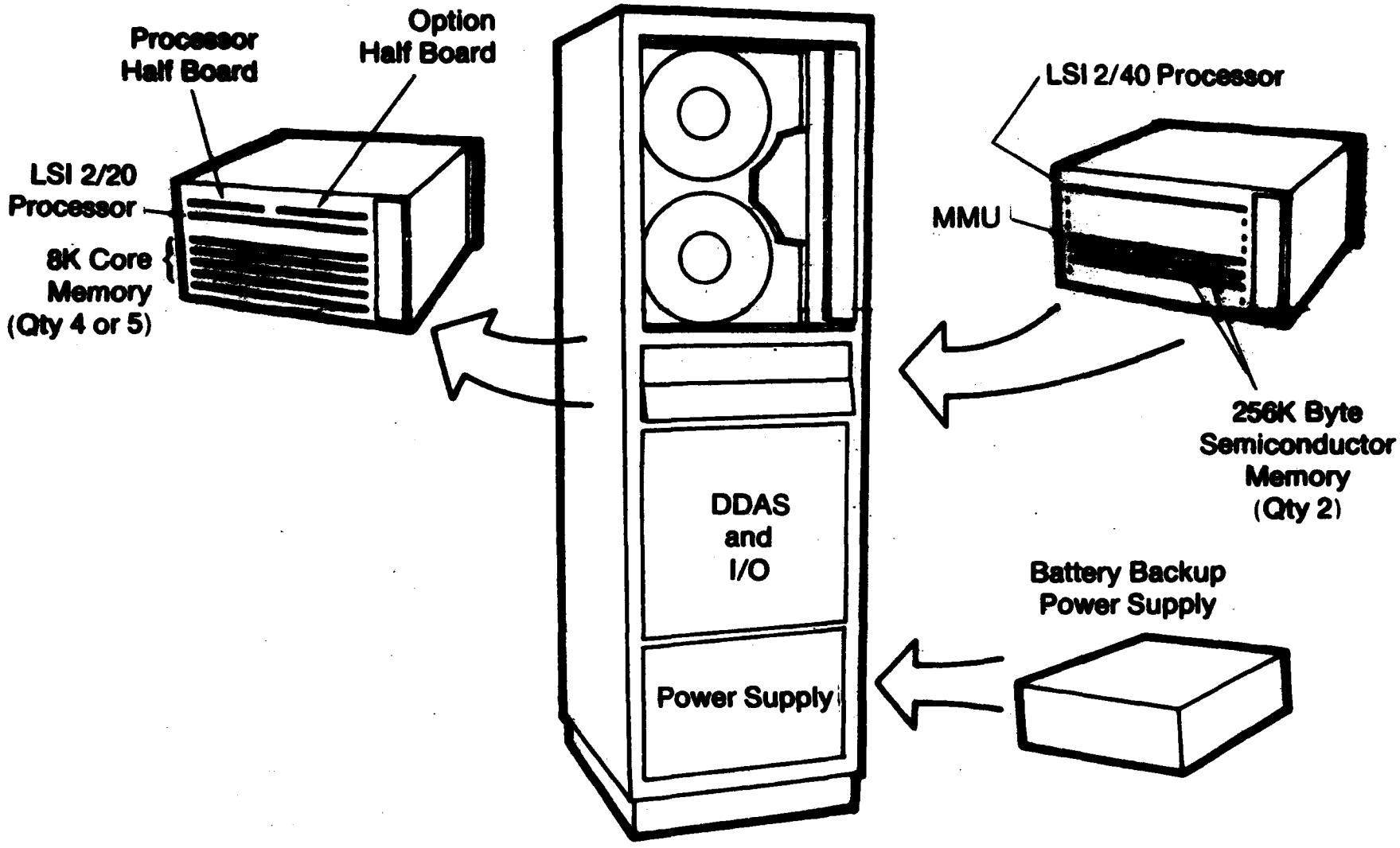


FIGURE 16, ARTS IIA EQUIPMENT INSTALLATION

State-of-the-art advances consisting of fewer and more reliable components are expected to improve overall processor reliability. The 2/40 has several high-level languages that should be explored for use in developing the safety enhancements. Increased memory availability will allow the substitution of memory use for CPU cycles and free the processor from some functions.

Cost and Scheduling

Adding an LSI-2/40 is expected to be the lowest cost alternative. Code transportability will lower development costs; ease of implementation and similarity to current equipment will lower training costs. Hardware compatibility eliminates the need for costly additional interfaces.

A preliminary system development cost estimate has been prepared, including software development for the near-term enhancements. Figure 16 is an estimated software development schedule based on the production of 18,000 lines of code. A total of 486 person-months are required for the individual software development tasks in Table 3. A cost of $6,250 per person-month was used in software development estimates.

In addition to software development, system development costs include:

- Hardware development of the battery backup power supply and aural alarm (40 person-months--$250,000).
- Program management (24 person-months--$150,000).
- Support (40 person-months--$200,000).

Thus, we estimate a total of $3.6 million in development costs. This estimate, when discounted to 1980 dollars from 1982 dollars (the expected midpoint of the development effort), yields a cost of $2.975 million.

Once the safety enhancement package has been developed, a training course must be developed for use in Oklahoma City to train the data systems specialist at each site. The cost of setting up the original ARTS II Training course was approximately $500,000. This course included maintenance and data systems specialist (DSS) training. A

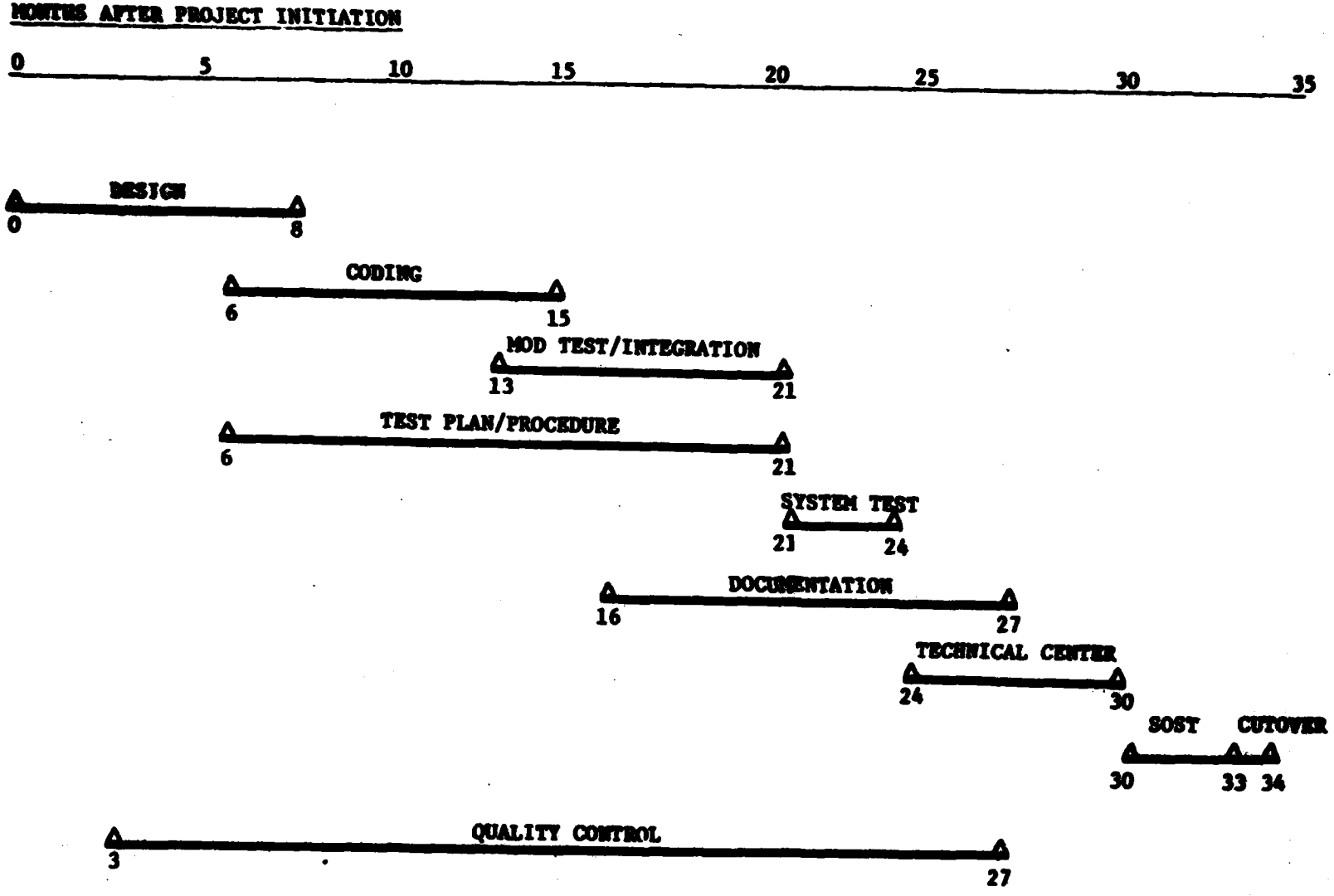


FIGURE 16 SOFTWARE DEVELOPMENT SCHEDULE

modified training course for the ARTS II enhancements and new hardware is estimated at $100,000. In addition, it will cost approximately $5,000 per site to send a DSS to Oklahoma City for several weeks of training.

Table 3

TIME ALLOCATIONS FOR SOFTWARE DEVELOPMENT TASKS

Task	Person-Months
Design	45
Coding	113
Modular test/integration	76
Test plan/procedure	50
System testing	30
Documentation	76
Technical center	48
Site operational system test	21
Cutover	4
Quality control	23
Total	486

The list price of the replacement 2/40 computer has been estimated at $16,800 per system. This cost includes:

- A 2/40 processor board
- Memory management unit (MMU)/cache memory board
- Two 256K-byte memory boards (ECC RAM semiconductor memory)
- A 60-A power supply
- The required 9-slot "split" chassis.

The 9-slot split chassis is the same size and requires the same mounting as the present chassis. An optional Autoload ROM, which is also needed to match existing specifications, plugs into the processor board and costs an additional $100.

Another requirement for the new processor is sufficient memory backup to keep the system current for short power failures. Engineering development work for the backup power supply has been included in development

costs. The backup power supply is expected to be mounted in the same position as the current power supply.

It is assumed that one spare of each board (at $9,500) must be purchased for each site and that a 25% markup will be made on all hardware. Thus, the estimated hardware cost is $21,000 per site, plus a spare cost of $12,000 per site.

Although the installation site preparation for the initial ARTS II start-up was expensive, the major cost of installing ARTS II enhancements will be a simple change of computer hardware and power supplies. Because current and upgraded processor and power supply chassis are the same size, no major effort or site modification should be required.

The cost of installation at an average site is estimated at $8,000. This figure, at half the cost of the original ARTS II installation, is considered conservative. The expected cost of hardware, spares, and installation is $41,000 per site.

The year 1985 has been used as the time of hardware purchase and installation, assuming installation follows a 3-year development effort. These costs for 90 sites, discounted to 1980 dollars, are $2.3 million. The 1980 cost will be higher if hardware purchase takes place before, and independently of, software development.

At each site, there are recurring maintenance costs for labor and parts. Annual parts usage has been estimated at 25% of the spares, on an average cost of $3,000 per site. The cost of maintenance labor is not expected to increase.

The total estimated cost for the recommended alternative is $6.7 million (discounted to 1980 dollars). These figures are summarized in Table 4.

Risks and Additional Information

Although several factors point to the use of the LSI-2/40 as a replacement computer, a number of risks should be explored before any commitments are made. LSI-2/40 uncertainties include:

Table 4

COST ANALYSIS OF RECOMMENDED ALTERNATIVE

	Common (thousands of dollars per year)	Per Site (thousands of dollars per year)	Year	Total (thousands of 1980 dollars)
One-time costs				
System development				
Software development (486 person-months)	3,000			
Hardware development	250			
Program management	150			
Program support	200			
Total	3,600		1982	2,975
Training for maintenance	100	5	1984	375
Equipment purchase				
Hardware		21		
Spares		12		
Implementation		8		
		41	1985	2,291
Recurring costs				
Maintenance and parts	Base	3	1985	1,089
Labor	Base			
Total				6,730 or $6.7 million

- Availability and support from Computer Automation
- Semiconductor memory
- Code transportability
- Processor capacity
- Hardware reliability.

A number of 2/40s have been made at Computer Automation, and a production run of 50 is now completed and in testing. Production will be in batches of 50 as dictated by demand. It is suggested that the progress of 2/40 production at Computer Automation be closely monitored in the coming months.

It has been FAA policy to require nonvolatile core memory in ATC systems to ensure the integrity of data through short power interruptions. The 2/40's Cache/Memory Mapping Unit requires the use of volatile semiconductor memory. This type of memory has been chosen because of its cost, speed, and greater capacity. To ensure the retention of data through power transitions, a backup battery power supply must be developed for use with the new processor. Computer Automation plans to develop such a power supply for delivery in 6 to 9 months. We recommend that detailed information be sought on the battery backup and that its development be closely monitored to ensure timely availability and a match with ARTS IIA requirements.

The 2/40 has been designed and marketed to provide complete code compatibility between the two processors. This assumption, which has been crucial in choosing the 2/40 as a replacement, must be validated by benchmarking an ARTS II code run on a 2/40 processor with an APC receiving synthetic DDAS data.

Few data are available on the new processor's capacity to actually run ARTS II and ARTS IIA applications. It is assumed that the 2/40 will run 2 to 2.5 times faster than the 2/20 and that the safety functions can be handled by one 2/20. Estimates of the processing and memory requirements of the safety enhancements should be made, and tests should then be performed with the 2/40 to determine its adequacy.

No reliability estimates have yet been made for the 2/40 processor. It is assumed that it will provide better availability than the 2/20 because of advances in manufacturing technology and because of the reduced number of boards required. It is recommended that the vendor make MTBF estimates or that a test be conducted on the full ARTS II hardware with an installed 2/40 processor.

In summary, the LSI-2/40 has been chosen as a replacement computer for the LSI 2/20 because of system compatibility that will allow:

- Lower development costs.
- Code transportability.
- Minimum site disruption.
- System capacity to provide for safety enhancements with a processor the same size as the current one.
- Lower cost because of:
  - Low hardware and interface costs.
  - Lower development costs because of the ease of code transportability and simplicity in the upgrade.

VII LONG-TERM DEVELOPMENTS

As currently envisioned, ARTS IIA consists of additional and replacement hardware, and additional software for the operational program. The hardware is a newer, faster computer, larger and faster semiconductor memory, a battery backup power supply to maintain memory contents in case of power failure, and aural alarm equipment for CA and MSAW. The software added to the operational program consists of a beacon tracker, algorithms for CA and MSAW, and TTG. In addition, various nonoperational programs will be written to facilitate site adaptation of MSAW data and the writing of scenarios for TTG. These near-term enhancements assume input from ATCBI equipment of the current series, and primary radar with video input (e.g., ASR-7). Also, current ARTS II RADS are to be used.

A variety of new equipment is anticipated for use in ATC systems. When applied to ARTS II, these devices can be divided into two categories: digital and other input (i.e., aircraft sensing) devices, and various output devices (i.e., displays and postprocessors). Each of these categories has an effect on the life-cycle scenario of ARTS IIA as currently configured.

Input Devices

The basic effect on ARTS IIA of newer and more powerful sensing devices is to reduce the workload of the ARTS IIA computer. Such devices (e.g., DABS and SRAP) produce target reports and allow the elimination of the ARTS II SWEEP program, which is currently performing target declaration. They will also perform tracking and correlation. This will reduce the workload of the computer, because the direct input of track numbers to the computer will reduce the amount of searching currently being done to determine if a target entry is already established. In addition, DABS will perform MSAW and CA computations. The net effect

of these facilities will be to make the development of the near-term safety enhancements discussed in this report an interim measure until anticipated hardware is implemented at ARTS sites. It is, however, recommended that these enhancements be made; they can be implemented at ARTS II sites long before the installation of additional, more advanced equipment. Furthermore, it will be a relatively simple matter to decommission the SWEEP program, once its functions are performed elsewhere.

Output Devices

Common characteristics of anticipated output devices such as FDAD and TCDD are their digital input format (i.e., non-time-shared) and their ability to self-refresh. Although the input specifications of FDAD are not finalized, FDAD will allow the ARTS computer to output change data only, greatly reducing the amount of data sent to the displays. The self-refresh capability, similar to that of the Tampa ARTS IIIA system's MDBMs, will also reduce the cycle-stealing required by the ARTS II DMA. Utilizing these features will require some reprogramming of the refresh sections of the ARTS II operational program; the net effect will be reduced workload.

One ATC system not fitting into the input/output definition is TIDS. TIDS is not yet well specified enough for a dicussion of its total effect on the ARTS II system. For instance, it is not known whether TIDS will make any demands on the RADS or BANS subsystems. Such demands, of course, would require major changes in hardware and programming. The most likely scenario is of a TIDS-ARTS IIA computer-to-computer interface for the purpose of message transaction processing. The frequency and size of these messages are considerably less than the primary ARTS II target processing and display servicing functions and are expected to have little effect on the operational program or workload. There will be need for reprogramming to handle messages and to access the ARTS II data base.

The anticipated implementation of these devices does not invalidate the ARTS IIA configuration recommended here. In fact, use of these

devices will reduce the workload imposed on the ARTS IIA computer--a workload that is now being increased as a result of the near-term enhancement algorithms. This has the effect of reducing the long-term risk involved with the as-yet unproven speed of the Computer Automation LSI-2/40 that would run the ARTS IIA application. Therefore, there are no long-term difficulties anticipated in the long-term use of the ARTS IIA system, once the hardware and software recommendations of this report are implemented. ARTS IIA is expected to have a life scenario consistent with other ATC systems.

VIII SUMMARY AND CONCLUSIONS

The current ARTS II computer (a Computer Automation LSI-2/20) is currently fully utilized for existing functions under heavy traffic and maximum configuration conditions; consequently, more capacity (speed and memory size) is required to perform the near-term safety enhancement functions. These enhancements--MSAW, CA, beacon target tracking, and TTG--are candidates for early implementation at ARTS II sites. Therefore, there is a need to upgrade the computer to accommodate these and future enhancements as well as allow for growth in air traffic.

Our main conclusion is that the existing LSI-2/20 should be replaced with the larger, faster LSI-2/40, a new offering from Computer Automation. The LSI-2/40 can be installed in the same cabinet space with a simple chassis change, and is upgrade-compatible with the current computer. That is, current LSI-2/20 programs are expected to run without any modification on the new LSI-2/40 computer, and the current I/O controllers and interfaces can be immediately and directly attached to the LSI-2/40. Further, the LSI-2/40 is 2 to 2.5 times faster and has a memory expansion capability of up to 1 Megabyte in the existing chassis. The initial configuraiton should contain 512K bytes of low-cost semiconductor memory.

Generally, the major LSI-compatible alternatives, such as adding another LSI-2/20 or adding slave LSI-4/10S processors, have severe speed and memory limitations. The non-LSI-compatible alternatives, such as adding or replacing the existing computer with an incompatible computer, have significant disadvantages when compared with the LSI-2/40. Such alternatives were more expensive, required difficult and costly implementation, required the development of new interfaces and functional partitioning, and/or required redeveloping the current software for the new computer.

We considered the effects on cost and development decisions of possible future upgrades to provide redundancy and allow the use of digital displays, digital input, and correlated radar inputs. Undefined future requirements (e.g., DABS interface), specifications, and technologies outweigh any cost advantages of providing in advance for possible far-term enhancements.

We concluded that the best alternative was to implement only the required near-term enhancements, with the faster, larger LSI-2/40 replacing the LSI-2/20. This alternative, of course, still provides a basis for later far-term enhancements. It also provides for separate expansion of the hardware and development of enhancement software. Advantages are:

- Ease of implementation
- No site modifications
- Simple equipment change
- Little impact on operations
- Compatible and familiar equipment family.

The hardware can be installed quickly and before any software modifications in order to satisfy current demands for more capacity and verify the hardware concept. Burroughs, as the original developer of the ARTS II system, has in-depth experience and expertise that can be used to substantially shorten the implementation time and reduce the cost.

The hardware expansion consists almost entirely of off-the-shelf components, and can proceed contingent on:

- Validation and verification of the compatibility, performance, capacity, and reliability of the LSI-2/40.
- Validation and verification of the capabilities of a new power supply with an integrated backup battery providing for retention of the contents of the LSI-2/40's semiconductor memory during power line transients, including power failures of short duration.
- Validation and verification of code transportability.

These activities should begin as soon as possible. The power supply is not yet commercially available as an off-the-shelf component, but will probably be available by the time FAA has prepared the necessary

contracts. In-house development of the power supply by Burroughs is an acceptable alternative. The hardware specifications (Appendix C) establish the detailed requirements for these components. They also specify an aural alarm subsystem that must be included in the hardware expansion, but may be installed concurrently with installation of the MSAW and CA safety enhancements.

The development, testing, and implementation of the software enhancements will take much longer to complete than the hardware expansion. It is estimated that about 2 years for development and testing of the software, and perhaps an additional year for acceptance, field testing, and final installation, will be required. These estimates are lower than earlier expectations due to the availability of suitable off-the-shelf hardware components and the continuation of the current ARTS II contractor.

Appendix A

ARTS II ENHANCEMENTS DESIGN ALTERNATIVE STUDY DOCUMENTS

Appendix A

ARTS II ENHANCEMENTS DESIGN ALTERNATIVE STUDY DOCUMENTS

ARTS II Instruction Book (Burroughs Corporation TI 6190.11, November 1977).

ARTS II Acquisition and Processing Set Manual (Burroughs Corporation TI 6190.12, November 1977).

ARTS II RADS Manual (Burroughs Corporation TI 6190.13, November 1977).

ARTS II BRITE Manual (Burroughs Corporation TI 6190.14, November 1977).

ARTS II Magnetic Tape Unit Equipment Manual (Burroughs Corporation TI 6190.15, November 1977).

ARTS II Computer Equipment Manual (Burroughs Corporation TI 6190.16, November 1977).

ARTS II Television Camera Equipment Manual (Burroughs Corporation TI 6190.17, November 1977).

ARTS II Operational Program Reference Manual (Burroughs Corporation TI 6190.18, November 1977).

ARTS II Operational CPFS (Burroughs Corporation TI 6190.19, November 1977).

ARTS II Operational Program Operator's Manual (Burroughs Corporation TI 6190.21, November 1977).

ARTS II Diagnostic and Maintenance Program Reference Manual (Burroughs Corporation TI 6190.22, November 1977).

ARTS II Utility Program Reference Manual (Burroughs Corporation TI 6190.23, November 1977).

ARTS II Coding Specifications (AAT-550, Version A2.01, October 1978).

ARTS II Design Data (Burroughs Corporation 33300-74-2641, February 1977).

ARTS III Beacon Tracking Level (BTL) System Specificiations.

ARTS III Coding Specifications (FAA, 77-0291-4, July 1977).

ARTS III CPFS (AAT-550, NAS-MD-601 through 615, July 1977).

ARTS III Design Data: Beacon Radar Tracking.

ARTS III Design Data: Conflict Alert Stage 1 (Sperry Univac ATC 10410, December 1976).

ARTS III Design Data: MSAW (Sperry-Univac, PX-11325, March 1976).

ARTS III General System Manual for Beacon Tracking Level System (Sperry-Univac, PX 6213, October 1971).

ARTS III Operational Program Assembly Listing.

ARTS IIIA Tampa/Sarasota CPFS (Sperry-Univac, ATC 10719, October 1978).

Terminal Area Forecasts 1979-1990 (FAA-AVP-78-6, June 1978).

TIPS: ARTS III Input/Output Requirements (MITRE MTR-7161, November 1976).

Appendix B

AIR TRAFFIC AT ARTS II SITES

The following pages describe current traffic and projected traffic at 75 ARTS II sites included in "Terminal Area Forecasts, Fiscal Years 1979-1990," June 1978, FAA-AVP-78-6.

The first line of each entry shows the site name and airport location identifier. The next three lines show traffic projections for 1979 and 1990 and the percentage increase. Traffic projections are given as three figures: number of total operations handled, number of instrument operations in thousands, and the total approaches handled. Total aircraft operations is defined as the sum of itinerant and local operations. An aircraft operation is counted for both a landing and a takeoff. Instrument operations occur when an FAA-operated terminal-control facility handles the arrival, departure, or overflight of an IFR aircraft or provides IFR separations to other aircraft. The figures include instrument operations at primary and secondary facilities. Total approaches is the total of all instrument approaches.

	TOTAL OPS. (1000'S)	INST. OPS. (1000'S)	TOTAL APPR.
EDWARDS	**EDW**		
1979	1	139	1
1990	1	197	1
%	0	41	0
LUBBOCK	**LBB**		
1979	153	188	1860
1990	199	251	2526
%	30	33	35
TOLEDO	**TOL**		
1979	132	155	6362
1990	170	237	8319
%	28	52	30
PENSACOLA	**PNS**		
1979	128	211	2123
1990	158	301	2755
%	23	42	29
KNOXVILLE	**TYS**		
1979	162	160	4579
1990	211	246	6114
%	30	53	33
FORT-WAYNE	**FWA**		
1979	167	140	4432
1990	219	215	5949
%	31	53	34
ANCHORAGE	**ANC**		
1979	309	100	5490
1990	400	155	8171
%	29	55	48

		TOTAL OPS. (1000'S)	INST. OPS. (1000'S)	TOTAL APPR.
FAIRBANKS	FAI			
1979		226	42	934
1990		324	62	1403
%		43	47	50
SPOKANE	SKA			
1979		1	145	1
1990		1	207	1
%		0	42	0
W-PALM-BCH	PBI			
1979		243	233	2474
1990		320	361	3232
%		31	54	30
MACON-ROBBINS	MCN			
1979		66	148	2081
1990		87	218	2778
%		31	47	33
GRIFFIS-ROME	RME			
1979		1	62	1
1990		1	91	1
%		0	46	0
LITTLE-ROCK	LIT			
1979		176	213	4853
1990		222	319	6738
%		26	49	38
DULUTH	DLH			
1979		85	46	2543
1990		106	68	3279
%		24	47	28

	TOTAL OPS. (1000'S)	INST. OPS. (1000'S)	TOTAL APPR.
DAYTONA	DAB		
1979	306	58	3088
1990	394	89	3954
%	28	53	28
BURLINGTON	BTV		
1979	118	135	1999
1990	153	199	2771
%	29	47	38
COLORADO-SPRGS		COS	
1979	215	157	1429
1990	271	244	1911
%	26	55	33
AKRON	CAK		
1979	174	169	6292
1990	221	256	8295
%	27	51	31
HARRISBURG	CXY		
1979	170	122	3283
1990	215	167	4293
%	26	36	30
WILKES-BARRE	AVP		
1979	88	37	7314
1990	115	56	11372
%	30	51	55
BEAUMONT	BPT		
1979	129	33	2379
1990	175	51	3514
%	35	54	47

	TOTAL OPS. (1000'S)	INST. OPS. (1000'S)	TOTAL APPR.
ALLENTOWN	ABE		
1979	164	59	8806
1990	224	90	13318
%	36	52	51
EVANSVILLE	EVV		
1979	109	64	2621
1990	141	94	3456
%	29	46	31
TALLAHASSEE	TLH		
1979	118	53	3126
1990	157	82	4277
%	33	54	36
PORTLAND-ME	PWM		
1979	119	37	2771
1990	161	55	4194
%	35	48	51
SPRINGFIELD	SGF		
1979	111	40	1726
1990	213	61	2260
%	91	52	30
CHARLESTON	CHS		
1979	153	150	5804
1990	178	232	7175
%	16	54	23
LAKE-CHARLES	LCH		
1979	65	24	2283
1990	87	37	3406
%	33	54	49

		TOTAL OPS. (1000'S)	INST. OPS. (1000'S)	TOTAL APPR.
MUSKEGON	MKG			
1979		118	32	2938
1990		151	48	4220
%		27	50	43
WATERLOO	ALO			
1979		115	34	1350
1990		163	53	1835
%		41	55	35
PALM-SPRGS	PSP			
1979		115	18	58
1990		150	27	81
%		30	50	39
CASPER	CPR			
1979		118	21	1185
1990		157	33	1608
%		33	57	35
WILMINGTON	ILM			
1979		100	42	2250
1990		124	64	2939
%		24	52	30
CHAMPAIGN	CMI			
1979		185	52	2182
1990		238	78	2867
%		28	50	31
BANGOR	BGR			
1979		104	36	4118
1990		138	55	6358
%		32	52	54

	TOTAL OPS. (1000'S)	INST. OPS. (1000'S)	TOTAL APPR.
LAFAYETTE	LFT		
1979	184	50	2843
1990	264	76	4082
%	43	52	43
PUEBLO	PUB		
1979	134	34	468
1990	164	54	590
%	22	58	26
LONGVIEW	GGG		
1979	126	19	1756
1990	170	29	2563
%	34	52	45
GULFPORT	GPT		
1979	91	43	1754
1990	115	64	2469
%	26	48	40
MONROE	MLU		
1979	124	32	2931
1990	158	49	3903
%	27	53	33
ROCKFORD	RFD		
1979	244	68	4674
1990	314	101	6139
%	28	48	31
GREENSBORO	GSO		
1979	173	254	6166
1990	209	380	7989
%	20	49	29

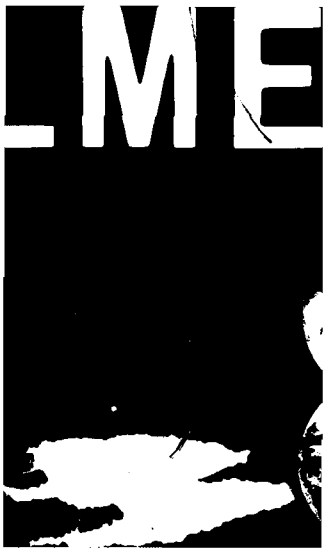
		TOTAL OPS. (1000'S)	INST. OPS. (1000'S)	TOTAL APPR.
WICHITA	ICT			
1979		298	223	6182
1990		430	336	8297
%		44	50	34
SAVANNAH	SAV			
1979		129	134	2529
1990		162	204	3256
%		25	52	28
RICHMOND	RIC			
1979		187	175	6049
1990		255	270	8386
%		36	54	38
CORPUS-CHRISTI	CRP			
1979		171	120	6068
1990		211	168	7615
%		23	40	25
HUNTSVILLE	HSV			
1979		112	120	3940
1990		145	180	5290
%		29	50	34
MOBILE	MOB			
1979		141	144	3809
1990		175	220	4867
%		24	52	27
MERIDIAN	MEI			
1979		62	2	1659
1990		73	3	2025
%		17	50	22

		TOTAL OPS. (1000'S)	INST. OPS. (1000'S)	TOTAL APPR.
JACKSON	JAN			
1979		98	75	5024
1990		127	112	6765
%		29	49	34
RENO	RNO			
1979		198	56	2106
1990		300	87	2795
%		51	55	32
ATLANTICCITY	ACY			
1979		152	60	2842
1990		218	90	3663
%		43	50	28
GREENVILLE	GMU			
1979		135	18	2108
1990		176	27	2821
%		30	50	33
BRISTOL	TRI			
1979		111	59	5669
1990		146	90	7840
%		31	52	38
CHATTANOOGA	CHA			
1979		147	134	4440
1990		194	208	5891
%		31	55	32
KALAMAZOO	AZO			
1979		140	56	3425
1990		181	81	4412
%		29	44	28

		TOTAL OPS. (1000'S)	INST. OPS. (1000'S)	TOTAL APPR.
WACO	ACT			
1979		88	31	1451
1990		125	46	2488
%		42	48	71
READING	RDG			
1979		182	24	3466
1990		248	37	5188
%		36	54	49
ROANOKE	ROA			
1979		149	86	5508
1990		196	128	7170
%		31	48	30
SOUTH-BEND	SBN			
1979		125	164	4659
1990		166	241	6479
%		32	46	39
SPRINGFIELD	SPI			
1979		182	113	2993
1990		230	174	3844
%		26	53	28
SANTA-BARBARA	SBA			
1979		237	29	3847
1990		317	45	5648
%		33	55	46
BAKERFIELD	BFL			
1979		186	45	3888
1990		247	69	5212
%		32	53	34

		TOTAL OPS. (1000'S)	INST. OPS. (1000'S)	TOTAL APPR.
HILO	ITO			
1979		65	28	4336
1990		84	44	5514
%		29	57	27
CLARKSBURG	CKB			
1979		84	44	2255
1990		118	61	3783
%		40	38	67
TERRE-HAUTE	HUF			
1979		107	33	1733
1990		146	50	2795
%		36	51	61
MANCHESTER	MHT			
1979		152	31	2410
1990		199	46	3414
%		30	48	41
EUGENE	EUG			
1979		187	39	4330
1990		240	58	5549
%		28	48	28
COLUMBIA	CAE			
1979		154	152	4653
1990		202	235	6221
%		31	54	33
FLORENCE	FLO			
1979		76	10	1644
1990		100	16	2313
%		31	60	40

	TOTAL OPS. (1000'S)	INST. OPS. (1000'S)	TOTAL APPR.
BISMARCK	BIS		
1979	94	20	1350
1990	122	31	1783
%	29	55	32
MANSFIELD	MFD		
1979	104	42	2311
1990	139	64	3226
%	33	52	39
STOCKTON	SCK		
1979	185	43	2634
1990	234	64	3367
%	26	48	27
FT-MYER	FMY		
1979	126	39	1029
1990	165	57	1435
%	30	46	39
GREAT-FALLS	GFA		
1979	1	39	1
1990	1	52	1
%	0	33	0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